PCI Express®
OCuLink
Specification
Revision 1.0

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1. Introduction to PCI Express OCuLink

This document is a companion Specification to the *PCI Express Base Specification* and other *PCI Express*® documents listed in *Section 1.1*. The primary focus of the *PCI Express OCuLink Specification* is the implementation of internal and external small form factor PCI Express® connectors and cables optimized for the client and mobile market segments. This Specification discusses cabling and connector requirements to meet the 8.0 GT/s signaling needs in the *PCI Express Base Specification*.

No assumptions are made regarding the implementation of PCI Express compliant components on either side of the Link; such components are addressed in other PCI Express Specifications.

1.1. Reference Documents

PCI Express Base Specification, Rev. 3.1 (*PCI Express Base* 3.1)

PCI Express Card Electromechanical Specification, Rev. 3.0 (*PCI Express CEM* 3.0)

PCI Express External Cabling Specification, Rev. 3.0

PCI Express Label Specification and Usage Guidelines, Rev. 1.1

EIA 364 Series, Electrical Connector Test Procedures Including Environmental Classifications with Test Procedures

EIA 364-1000, Environmental Test Methodology for Assessing the Performance of Connectors and Sockets used in Business Office Applications

SFF-8449 Management Interface for SAS

1.2. Documentation Conventions

1.2.1. Capitalization and Italicization

Some terms are capitalized or italicized to distinguish their definition in the context of this document from their common English meaning. Words not capitalized have their common English meaning. When terms such as *memory write* or *memory read* are shown completely in lower case, they include all transactions of that type.

Register names and the names of fields and bits in registers and headers are presented with the first letter capitalized and the remainder in lower case.

1.2.2. Numbers and Number Bases

Hexadecimal numbers are written with a lower case h suffix; (e.g., FFFh and 80h). Hexadecimal numbers larger than four digits are represented with a space dividing each group of four digits, as in 1E FFFF FFFFh. Binary numbers are written with a lower case b suffix; (e.g., 1001b and 10b). Binary numbers larger than four digits are written with a space dividing each group of four digits, as in 1000 0101 0010b.

All other numbers are decimal numbers.

1.2.3. Implementation Notes

Implementation Notes should not be considered to be part of this Specification. They are included for clarification and illustration only.

1.3. Terms and Acronyms

Terms and Acronyms not defined in this section may be found in the *PCI Express Base Specification*, the *PCI Express External Cabling Specification,* or the *PCI Express Card Electromechanical Specification*. Table 1-1 lists terms and acronyms specific to this specification.

Table 1-1. Terms and Acronyms

Terms/Acronyms	Definitions
Auxiliary signals	Signals that are not defined in the *PCI Express Base Specification,* but are necessary for certain desired functions or system implementation.
Back-Plane (BP) Type	A method to detect the end point interface type
Cable port	The connectors and signals associated with a specific x4 physical interface.
Fixed	Used to describe the gender of the mating side of the connector that accepts its mate upon mating. This gender is frequently, but not always, associated with the common terminology "receptacle". The term "Fixed" is adopted from EIA standard terminology as the gender that most commonly exists on the Fixed end of a connection.
Free	Used to describe the gender of the mating side of the connector that penetrates its mate upon mating. This gender is frequently, but not always, associated with the common terminology "plug". The term "Free" is adopted from EIA standard terminology as the gender that most commonly exists on the Free end of a connection.
Full Crossover	A pinout that connects all A side contacts to all B side contacts enabling mass termination of the cable.
Lane	One PCI Express Lane contains a differential pair for Transmit and another differential pair for Receive. A xN Link is composed of N Lanes.
Link	A collection of one or more PCI Express Lanes, providing the communication path between an Upstream and Downstream Port.
OCuLink	A small form factor Optical or Copper x4 PCI Express cable Link, targeting mobile and systems with small faceplate areas, for both external and internal cabling.
Port aggregation	The ability to aggregate multiple connectors to provide an equivalently larger connector (e.g., the ability to aggregate two or four x4 connectors to construct x8 or x16 equivalent connectors).
Sideband signaling	A method for signaling Link events and conditions using physical signals that are separate from those signals which form the main data Link between two components.
Subsystem	In the context of this Specification, Subsystem is a generic term, identifying either an Upstream or Downstream device, providing a cabled PCI Express Port.
VSP	Vendor-specific Position

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2. PCI Express OCuLink Overview

The *PCI Express OCuLink Specification* is intended to augment the PCI Express Specification suite to target specific usage models not addressed by the *PCI Express External Cabling Specification*. The PCI-SIG will provide appropriate education and guidance to enable members and the industry to determine which Specification will best meet their needs for a given application. The two Specifications will continue to independently evolve as the members and industry require. The *PCI Express OCuLink Specification* is focused on PCI Express cable solutions targeting, but not limited to, small form factor client and mobile external enclosures and internal enclosure solutions.

This Specification covers the following information:

- Cable and connector mechanical and electrical Specifications.
- Passive and Active cable Specifications.
- Peripheral power Specification.
- External enclosure cable Hot-plug.
- Sideband signaling and usage models.

2.1. Mechanical Overview

The mechanical Specification includes what is required to provide interoperable, properly operating, small form factor connectors and cable assemblies. All other aspects will be left to the industry to determine. The mechanical attributes include:

- Small form factor connector targeting small form factor enclosures or enclosures with limited faceplate area.
- Minimal connector size.
- At least four (4) connectors to fit within an area equivalent to the defined edge of a single-slot, full height add-in card faceplate.
- At least two (2) connectors to fit within an area equivalent to the defined edge of a single-slot, low profile add-in card faceplate.
- Minimal number of signal pins for the PCIe Link.
- Minimal number of sideband/auxiliary signal pins.
- Single connector form factor specification for both external and internal enclosures /applications.
- Mechanical retention, optionally passive or active, at both ends of the cable.
- Insertion/removal cycles equivalent to similar industry standard connectors:
    - External connectors must support a minimum durability of 10,000 insertions and removals;
    - Internal connectors must support a minimum durability of 50 insertions and removals.
- Symmetrical connector Specification (i.e., the same connector is used for both ends of a given cable).

- Single mechanical connector that enables any one of x1, x2, or x4 PCIe Lanes.
  An implementation is permitted to support any one of single x1, x2, or x4 PCIe Links.
- External cable Link Hot- plug enabled.
- Forward looking for future signaling levels – connector capable of supporting extrapolated PCI Express 4.0 signaling rates (currently targeting 16 GT/s) with reasonably sufficient margin.

2.2. Internal and External Cable Overview

2.2.1 Internal and External Cable scope

System cable interfaces intended to operate at PCIe Gen 3 (8.0 GT/s) must be designed to support both passive and active cables.

The types of OCuLink cable assemblies supported are outlined in the following sections.

2.2.1.1. Internal Cables

- Internal – Passive: No Power.
  See Table 3-1 and Table 3-2 for connector pinouts and Table 6-9 for cable layout.
- Internal – Active: 3.3 V per End, Optional 5 V Power not provided.
  See Table 3-1 and Table 3-2 for connector pinouts and Table 6-9 for cable layout.

2.2.1.2. External Cables

- External – Passive: Optional 5 V Power not provided.
  See Table 3-3 for connector pinout and Table 6-10 for cable layout.
- External – Active: 3.3 V per End, Optional 5 V Power not provided.
  See Table 3-3 for connector pinout and Table 6-10 for cable layout.
- External – Active: 3.3 V per End plus 5 V Power End to End.
  See Table 3-3 for connector pinout and Table 6-10 for cable layout.

2.3. Signal Description

Table 2-1. Signal Description

Signal	Description
PETp0, PETn0, PERp0, PERn0, PETp1, PETn1, PERp1, PERn1, PETp2, PETn2, PERp2, PERn2, PETp3, PETn3, PERp3, PERn3	Differential PCI Express Transmitter/Receiver Lanes (x4)
VSP	Vendor-Specific Position
CPRSNT#	Cable present signal
CWAKE#	Power management signal for Downstream device wakeup events.
PERST#	PCI Express Reset indicates when the applied main power is within the specified tolerance and is stable.
2-WIRE CLOCK	Management Bus Clock Internal applications must have 2-Wire Clock run down the cable end to end. External passive and active applications must have 2 Wire Clock terminated at the PCB and must not run down the cable end to end.
2-WIRE DATA	Management Bus Data Internal applications must have 2-Wire Data run down the cable end to end. External passive and active applications must have 2 Wire Data terminated at the PCB and must not run down the cable end to end.
3.3 V POWER	Power for the optional active cable circuitry (within the cable plug). External applications have optional implementations for +3.3 V. Internal applications have optional implementations for +3.3 V. (Vact = POWER 3.3 Vact TX, POWER 3.3 Vact RX). 3.3 V = Vman.
5 V POWER	External applications have optional end to end implementations for +5 V supplied by the root only.
All External OCuLink connectors require contacts for two power rails: +5 V and +3.3 V.	

See Appendix C and Appendix D for additional information for systems.

Auxiliary signals are provided on the connector to assist with system-level functionality or implementation. The PCI Express OCuLink cable connector and cabling support the following Auxiliary signals:

- CPRSNT# (required): Cable present detect, an active-low signal provided by a Downstream Subsystem to indicate that it is both present and its power is within tolerance.
  - Vman < 0.8 V ==> Low Level: Cable not present and/or power not applied
  - 1.4 V < Vman < 1.8 V ==> Middle Level: Cable present, but power not applied
  - Vman > 2.7 V ==> High Level: Cable present and power applied

- CWAKE# (required): Cable Wake, an active-low signal that is driven by a Downstream Subsystem to re-activate a PCI Express hierarchy's main power rails. Although optional for Upstream and Downstream Subsystems, all cable assemblies must include CWAKE#.
- PERST# (Required): PCI Express Reset.

- VSP (optional) Vendor-specific Position, function and implementation specified by vendor.

2.4. Signal Compatibility Matrix

- All auxiliary signals are required from a cabling perspective.
- The signals listed in Table 2-2 are for an Upstream and/or Downstream Subsystem, with a brief description of features enabled by it.

Table 2-2. Signal Compatibility Matrix

Signal	Type	Root / Downstream Subsystem	Cable Assembly	End Point / Upstream Subsystem	Comments
CPRSNT#	3.3 V Logic	Required Output	Required	Required Input	Required on both sides of the cable. The driver is open-drain type and requires high impedance during power off states. Possible states: High (3.3 V) and (3.3 V)/2.
CWAKE#	3.3 V Logic	Optional Input	Required	Optional Output	Optional on both sides of the cable. The driver is open-drain type and requires high impedance during power off states. Signal becomes bidirectional if both ends support OBFF.
PERST#	3.3 V Logic	Required Output	Required	Required Input	When negated indicates when the applied main power is within the specified tolerance and is stable. (Cable installed and power not applied).
VSP		Optional I/O	Required (Note 1,2,3,4)	Optional I/O	Optional on both sides of the cable, function specified by vendor, is permitted to be used to support legacy functions or future functionality.
BP TYPE		Optional Input	Required	Optional Output	Input required to enable a full crossover internal cable solution.

Notes:

1. The use of SMBus across the cable is an optional feature. This allows the use of cables that adhere to SFF-8449 for a PCI Express interface with a reduced feature set. Active Optical Cable assemblies may not want to implement SMBus across the cable for cost or complexity reasons, and therefore is permitted to have a reduced feature set. The Upstream Subsystems should not be designed in such a way as to require the use of SMBus across the cable. However, the SMBus controller is still required by both Upstream and Downstream fixed ends to read the cable assembly information for configuration of the PCIe devices that are part of the cabled Link.
2. It is recommended that systems employing VSP for REFCLK functionality utilize pins A12+/A13- for the ROOT and pins B12+/B13- for the ENDPOINT
3. SRIS architecture on Upstream and Downstream Subsystems is required if supporting no-wire VSP positions between Upstream and Downstream Subsystems
4. Verify systems enabling unshielded wire at VSP positions meet EMI emission and EMI susceptibility limits, as required by target market regulatory bodies.

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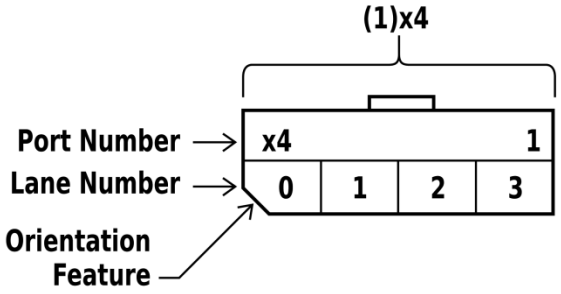
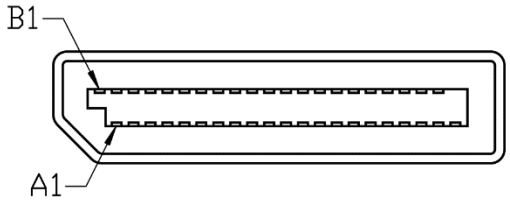
3. PCI Express Interconnect Overview

3.1. Lane Numbering and Pin Numbering for x4 Connector Solutions

Figure 3-1 displays the correct numbering of Lanes, with Lane numbers being incremented sequentially from the leftmost Lane position that contains pins labeled A1 and B1. Facing the same mating interface while in the same position, the connector pins are also numbered in sequential increments, left to right, in the direction away from the polarizing diagonal. This applies to both the vertical and right angle connectors in this Specification. The mating interface is also shown here for clarity.



Lane Numbering for x4 Interface



Pin Numbering for the x4 Fixed Board Mating Interface

Figure 3-1. Lane Numbering and Pin Numbering Locations for the x4 Fixed Connector Pinouts

3.2. Internal Connector Pinouts

3.2.1 Pinout for x4 Fixed Internal Connector (root)

- See Table 6-9 for the Full Crossover Internal Cable wiring.
- The sideband signal assignment differs between the root and end point.
- The Fixed side must provide the 3.3 V to support the optional active cable

Table 3-1. Pinout for x4 Fixed Internal Connectors (root)

Pin #	Description	Mating Sequence of cable to board		Pin #	Description
Row Offset – no pin this side			2nd	B1	RESERVED
A1	POWER 3.3 Vact RX	2nd	1st	B2	GROUND
A2	GROUND	1st	2nd	B3	PETp0
A3	PERp0	2nd	2nd	B4	PETn0
A4	PERn0	2nd	1st	B5	GROUND
A5	GROUND	1st	2nd	B6	PETp1
A6	PERp1	2nd	2nd	B7	PETn1
A7	PERn1	2nd	1st	B8	GROUND
A8	GROUND	1st	2nd	B9	2-WIRE CLOCK
A9	BP TYPE	2nd	2nd	B10	2-WIRE DATA
A10	CWAKE#	2nd	1st	B11	GROUND
A11	GROUND	1st	2nd	B12	PERST#
A12	VSP	2nd	2nd	B13	CPRSNT#
A13	VSP	2nd	1st	B14	GROUND
A14	GROUND	1st	2nd	B15	PETp2
A15	PERp2	2nd	2nd	B16	PETn2
A16	PERn2	2nd	1st	B17	GROUND
A17	GROUND	1st	2nd	B18	PETp3
A18	PERp3	2nd	2nd	B19	PETn3
A19	PERn3	2nd	1st	B20	GROUND
A20	GROUND	1st	2nd	B21	POWER 3.3 Vact TX
A21	RESERVED	2nd	Row Offset – no pin this side		

3.2.2 Pinout for x4 Fixed Internal Connector (end point)

- See Table 6-9 for the Full Crossover Internal Cable wiring.
- The sideband signal assignment differs between the root and end point.
- The Fixed side must provide the 3.3 V to support the optional active cable.

Table 3-2. Pinout for x4 Fixed Internal Connectors (end point)

Pin #	Description	Mating Sequence of cable to board		Pin #	Description
Row Offset – no pin this side			2nd	B1	RESERVED
A1	POWER 3.3 Vact RX	2nd	1st	B2	GROUND
A2	GROUND	1st	2nd	B3	PETp0
A3	PERp0	2nd	2nd	B4	PETn0
A4	PERn0	2nd	1st	B5	GROUND
A5	GROUND	1st	2nd	B6	PETp1
A6	PERp1	2nd	2nd	B7	PETn1
A7	PERn1	2nd	1st	B8	GROUND
A8	GROUND	1st	2nd	B9	BP TYPE
A9	2-WIRE CLOCK	2nd	2nd	B10	CWAKE#
A10	2-WIRE DATA	2nd	1st	B11	GROUND
A11	GROUND	2nd	2nd	B12	VSP
A12	PERST#	2nd	2nd	B13	VSP
A13	CPRSNT#	2nd	1st	B14	GROUND
A14	GROUND	1st	2nd	B15	PETp2
A15	PERp2	2nd	2nd	B16	PETn2
A16	PERn2	2nd	1st	B17	GROUND
A17	GROUND	1st	2nd	B18	PETp3
A18	PERp3	2nd	2nd	B19	PETn3
A19	PERn3	2nd	1st	B20	GROUND
A20	GROUND	1st	2nd	B21	POWER 3.3 Vact TX
A21	RESERVED	2nd	Row Offset – no pin this side		

3.3. External Connector Pinouts

3.3.1 Pinout for x4 Fixed External Connectors (root and end point)

- See Table 6-10 for x4 Free External Passive and Active Cable wiring.
- The sideband signal assignment is the same on the root and end point.
- The Fixed side must provide the 3.3 V to support the optional active cable.
- The Fixed side must provide the 5 V for optional Power.

Table 3-3. Pinout for x4 Fixed External Connector (root and end point)

Pin #	Description Root	Mating Sequence of cable to board		Pin #	Description
Row Offset – no pin this side			2nd	B1	POWER 5 V #1
A1	POWER 3.3 Vact RX	2nd	1st	B2	GROUND
A2	GROUND	1st	2nd	B3	PETp0
A3	PERp0	2nd	2nd	B4	PETn0
A4	PERn0	2nd	1st	B5	GROUND
A5	GROUND	1st	2nd	B6	PETp1
A6	PERp1	2nd	2nd	B7	PETn1
A7	PERn1	2nd	1st	B8	GROUND
A8	GROUND	1st	2nd	B9	2-WIRE CLOCK
A9	UNASSIGNED	2nd	2nd	B10	2-WIRE DATA
A10	CWAKE#	2nd	1st	B11	GROUND
A11	GROUND	1st	2nd	B12	PERST#
A12	VSP	2nd	2nd	B13	CPRSNT#
A13	VSP	2nd	1st	B14	GROUND
A14	GROUND	1st	2nd	B15	PETp2
A15	PERp2	2nd	2nd	B16	PETn2
A16	PERn2	2nd	1st	B17	GROUND
A17	GROUND	1st	2nd	B18	PETp3
A18	PERp3	2nd	2nd	B19	PETn3
A19	PERn3	2nd	1st	B20	GROUND
A20	GROUND	1st	2nd	B21	POWER 3.3 Vact TX
A21	POWER 5 V #2	2nd	Row Offset – no pin this side		

3.4. Port and Cable Aggregation

Note: These Ports are aggregated in the same order as Ports specified in the larger *PCI Express External Cable Specification*.

3.4.1. x4 Host and Peripheral Fixed Host Board-side Connector Aggregation

Host and peripheral Ports are permitted to be designed to support Port aggregation. A pair of x4 connectors that supports x8 Port aggregation are permitted t0 operate independently as x4 Ports, or be logically combined to form a single x8 Port. Similarly, a group of four x4 connectors that supports x16 Port aggregation are permitted to operate independently as x4 Ports, or be combined to form a single x16 Port. It is allowable for a pair of connectors to support x8 aggregation and also be part of a group that supports x16 Port aggregation.

- The x8 and x16 cables must provide the requisite number of x4 connectors at each end. The relative positioning of the individual x4 connectors must be such that they are able to be mated with the device connector pin and orientation arrangements defined in Figure 3-2 and Figure 3-3. The relative positioning and orientation of the connectors must be constrained enough to make it very difficult for a user to cross plug the connectors and achieve incorrect Lane ordering.
- When mated, the connector/cable set must not exceed the mechanical envelope defined by the Board-side connectors (see Chapter 9).

3.4.2. x4 Host and Peripheral Fixed Host Board-side Connector Aggregation Positioning Requirements

The basic Lane numbering and pin numbering for the Fixed-side is shown in Figure 3-1 for reference. The x4 Ports/connectors, x8 Ports/connectors, and the x16 Ports/connectors must be aggregated as shown in Figure 3-2 and Figure 3-3 for Board-side connectors as well as the marking/labeling requirements listed in Section 8.

The minimum distance between Fixed-side Ports in both X and Y directions is determined by the minimum pitch of the Free-side cable plug assemblies. Some of the reasons for this are:

- Application may require a larger gauge wire which makes the width of the plug wider and/or higher.
- Application may require a cable to exit from the side east or west or to exit north or south which would interfere with another Port in close proximity.
- Host is permitted to present the connectors with the connector orientation facing away from each other, or facing towards each other, which would affect finger clearance and spacing.

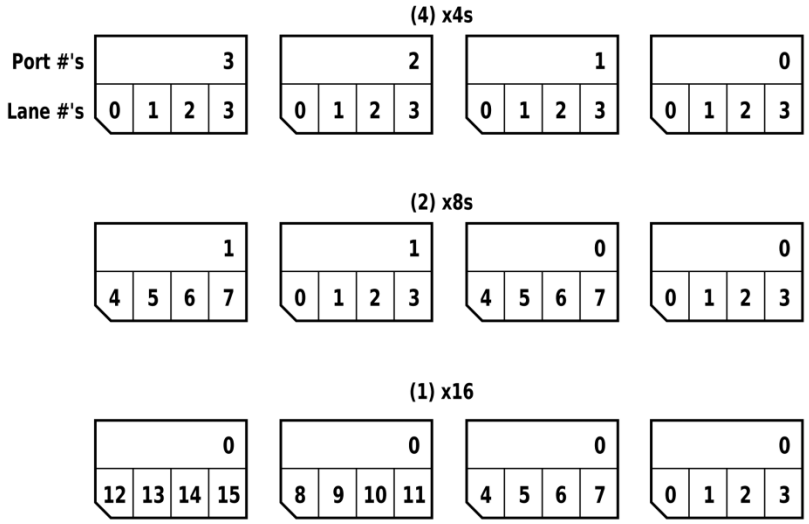


Figure 3-2. Port Aggregation for the x4 Fixed Host Board-side with Connector Orientation Facing the Same Direction

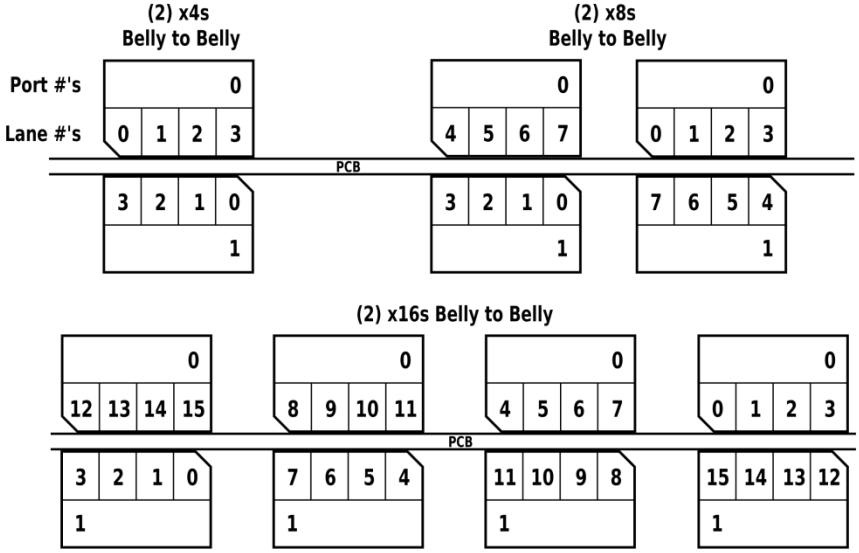


Figure 3-3. Port Aggregation for the x4 Fixed Board-side with the Connector Orientation Facing Away from Each Other

3.4.3. Additional Requirements for Aggregating Cables

- When mated, the connector/cable set must not exceed the mechanical envelope defined by the Fixed and Free connectors in this Specification.
- Cables are also permitted to be aggregated to match specific applications, where the host has aggregated Ports, or by request from an end user.
- See Chapter 8 for labeling requirements.
- See Appendix F for system level information pertaining to Port aggregation.

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4. x4 Fixed Host Board-side Connectors

- The x4 Fixed Host Board-side Connectors (see Figure 4-1 and Figure 4-5) are 42-contact SMT connectors with metal shells for robustness and for latching and are used for both external and internal applications.
- The x4 Free Cable connector, defined in Chapter 5 of this Specification, mates to the two Host Board-side connectors, defined in this section.
- The connectors accept both active and passive cable latching solutions, defined in Chapter 6 of this Specification.
- The connector shells are attached to the Fixed boards, by either intrusive reflow or SMT.

4.1. x4 Fixed Host Board-side Vertical Connector

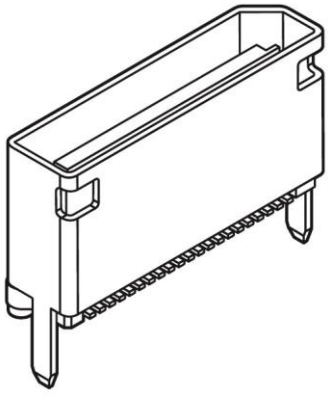


Figure 4-1. Isometric View of the x4 Fixed Host Board-side Vertical Connector

4.2. x4 Fixed Host Board-side Vertical Connector

Figure 4-2 shows the physical contact lengths for any configuration Fixed Side connector interface.

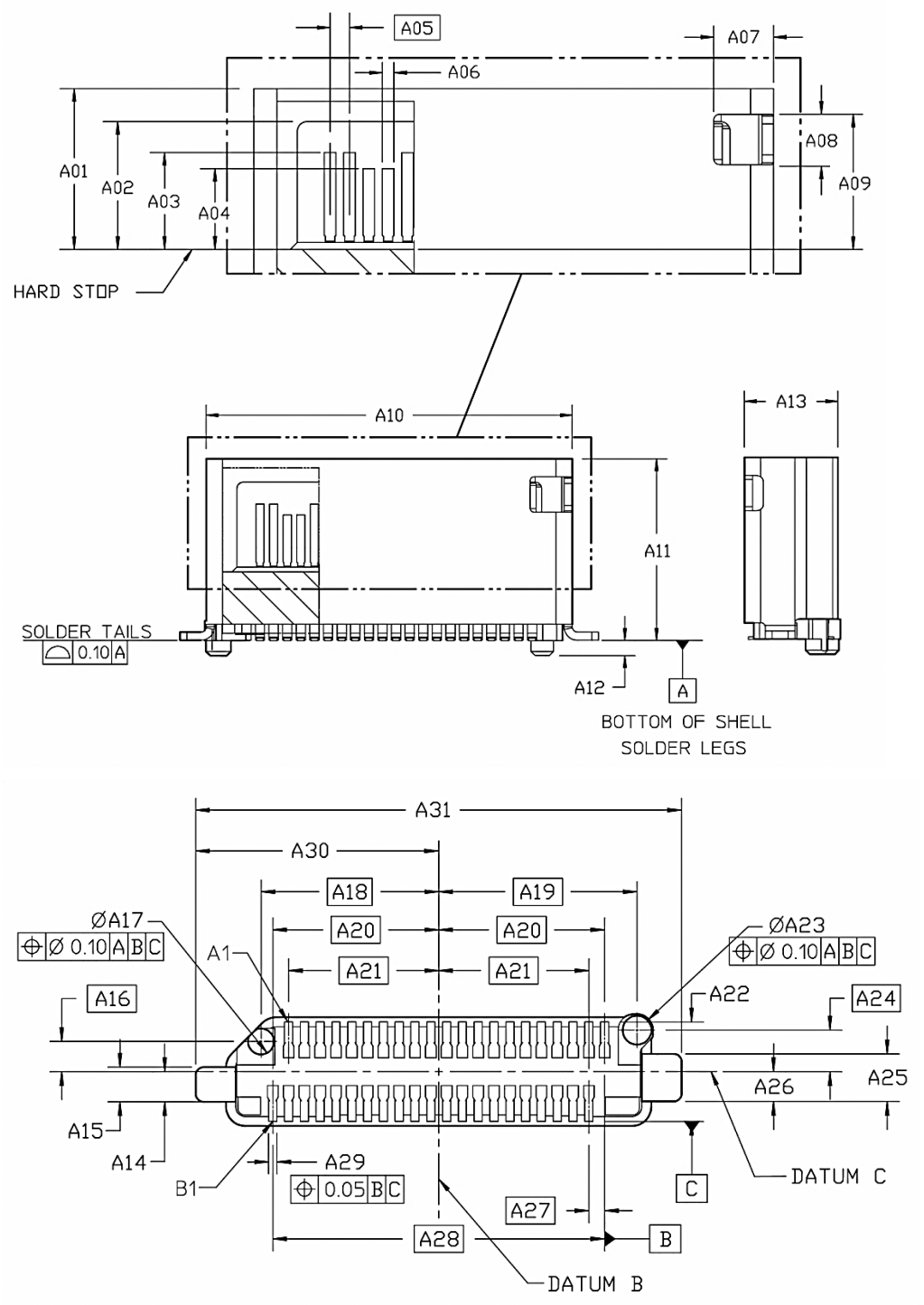


Figure 4-2. x4 Fixed Host Board-side Vertical Connector Form Factor Dimensions

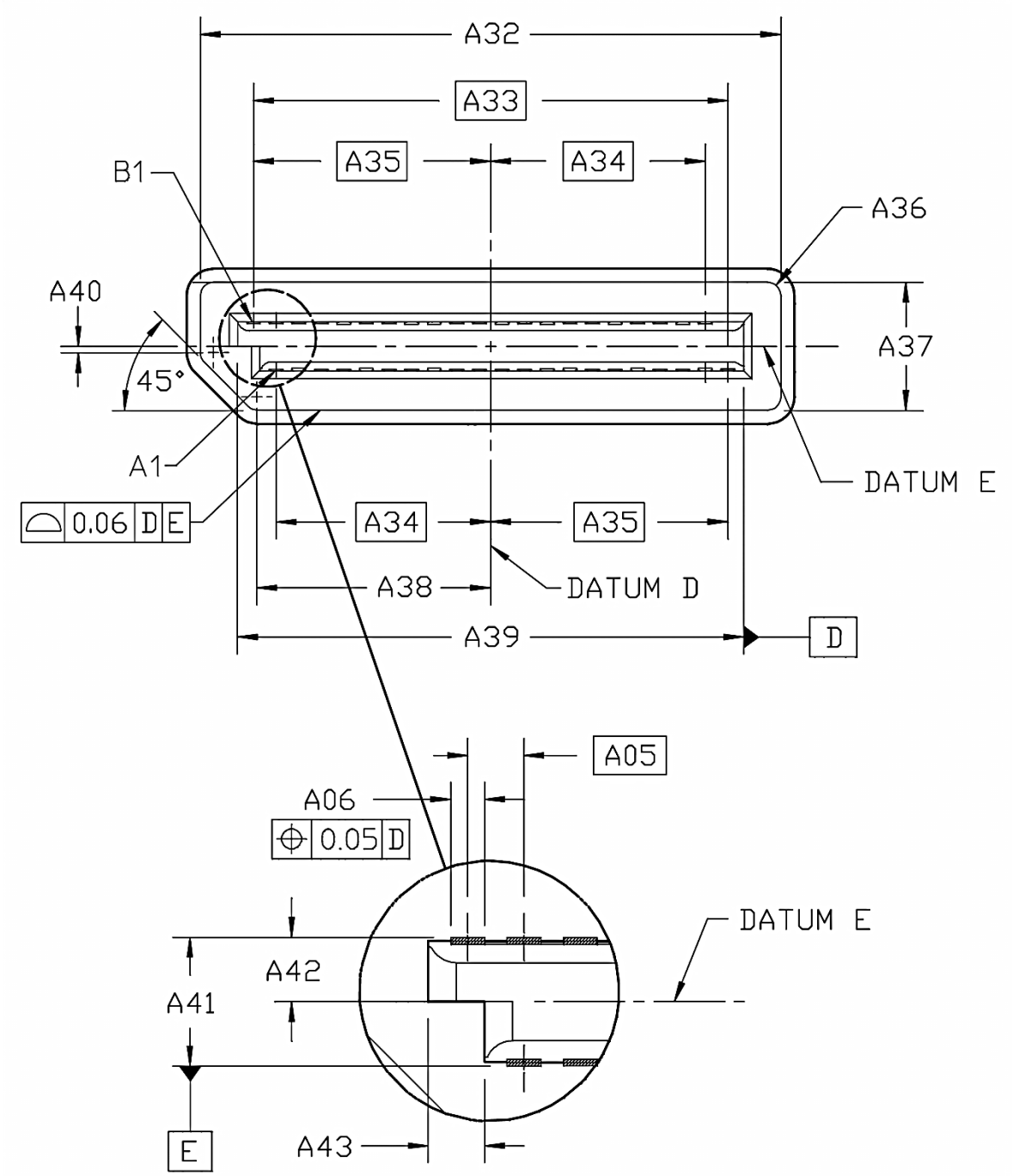


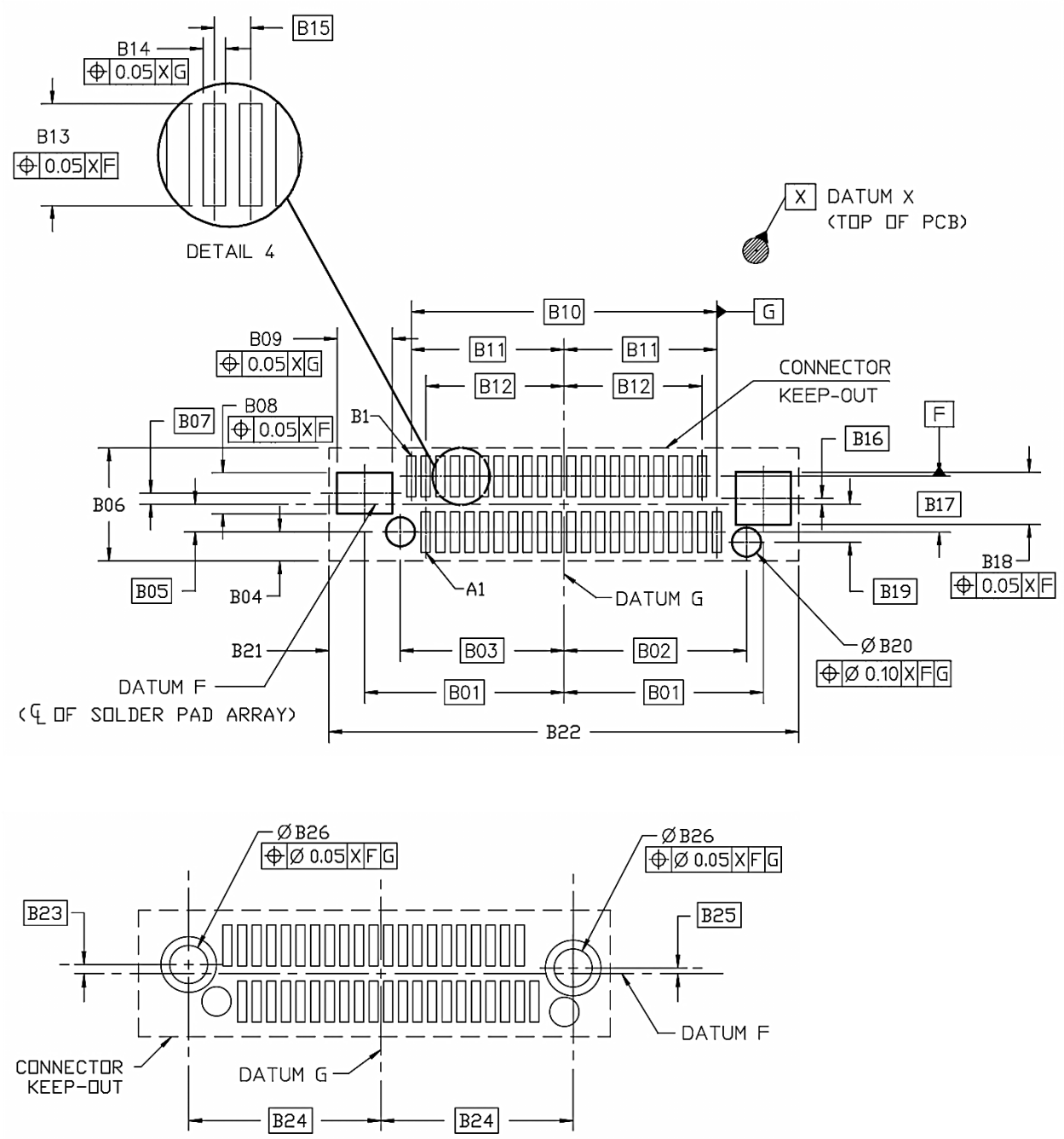
Figure 4-3. Mating Interface Dimensions for all x4 Fixed Host Board-side Connectors

Table 4-1. x4 Fixed Host Board-side Vertical Connector Dimensions

ID	Description	Dimension	Tolerance ±
Figure 4-2			
A01	Hard stop to front of shell	4.15	0.08
A02	Hard stop to interface paddle nose	3.30	0.03
A03	Hard stop to 1st mate contacts	2.42	0.12
A04	Hard stop to 2nd mate contacts	1.95	0.12
A05	Fixed connector contact beam pitch - Typical	0.50	Basic
A06	Fixed connector contact width - Typical	0.30	0.03
A07	Latch window width (2X)	1.55	0.08
A08	Latch window length (2X)	1.30	0.08
A09	Hard stop (housing) to latch point (shell) (2x)	3.49	0.11
A10	Connector (shell) overall length	13.45	Ref
A11	Connector (shell) overall height from bottom of shell solder legs (Datum A)	6.66	0.08
A12	Locating peg length (2X)	0.56	0.10
A13	Connector (shell) overall width	3.43	Ref
A14	Horizontal centerline (CL) of solder tail array (Datum C) to edge of small (left) solder leg of shell	0.95	0.19
A15	Small (left) solder leg (shell) width	1.09	0.10
A16	Horizontal CL of solder tail array (Datum C) to CL of inboard (left) locating peg (orientation feature end)	0.95	Basic
A17	Small (left) locating peg diameter	0.82	+0.03/- 0.15
A18	Vertical CL of solder tail array (Datum B) to CL of inboard (left) locating peg	5.62	Basic
A19	Vertical CL of solder tail array (Datum B) to CL of outboard (right) locating peg	6.28	Basic
A20	Vertical CL of solder tail array (Datum B) to CL of outside solder tails (long offset from Datum B) (2X)	5.25	Basic
A21	Vertical CL of solder tail array (Datum B) to CL of inside solder tails (short offset from Datum B) (2X)	4.75	Basic
A22	Edge of Row A solder tail contacts to edge of Row B Solder Tail Contacts. (Datum C)	3.14	0.16
A23	Large (right) locating peg diameter	0.97	+0.03/-0.15
A24	Horizontal CL of Solder Tail Array (Datum C) to CL of outboard/ large locating peg	1.31	Basic
A25	Large Solder Leg (Shell) width	1.50	0.10

ID	Description	Dimension	Tolerance ±
A26	Horizontal CL of Solder Tail Array (Datum C) to edge large right Solder Leg	0.94	0.19
A27	Solder Tail Contact pitch - Typical	0.50	Basic
A28	Outer solder tails CL to CL (lower left B1 to upper right A21) (Datum B)	10.50	Basic
A29	Solder tail width (solder pad contact area) - Typical	0.26	0.03
A30	Datum B to end of left solder leg of shell	7.69	0.05
A31	Length from end of left to end of right solder legs	15.38	0.10
Figure 4-3			
A32	Interface (inside shell) cavity width	12.85	0.03
A33	Outer contacts CL to CL (upper left B1 to lower right A21)	10.50	Basic
A34	Vertical CL of interface paddle length (Datum D) to CL inner terminals (2x) (short offset from Datum D)	4.75	Basic
A35	Vertical CL of interface paddle length (Datum D) to CL outer terminals (2x) (long offset from Datum D)	5.25	Basic
A36	Inside radius of Fixed connector Shell (5X)	0.30	0.05
A37	Interface (inside shell) cavity height	2.83	0.04
A38	Vertical CL of interface paddle length (Datum D) to inside shell radius	5.23	0.06
A39	Interface Paddle length	11.20	0.03
A40	Horizontal CL of interface paddle (Datum E) to inside shell radius	0.25	0.09
A44	Interface paddle length minus the orientation feature width	10.70	0.03
A41	Interface paddle thickness (over top of contact beams; plastic/paddle must be below top of contact beams)	1.08	0.06
A42	Orientation feature (on paddle) thickness	0.54	0.03
A43	Orientation feature (on paddle) width	0.48	Ref
A05	Fixed connector contact pitch (Repeated Dimension)	0.50	Basic
A06	Fixed connector contact width (Repeated Dimension)	0.30	0.03

1



Alternate Footprint for Shell Attach

Figure 4-4. x4 Fixed Host Board-side Vertical Connector Footprint

Table 4-2. Dimensions for x4 Fixed Host Board-side Vertical Contact Footprint

ID	Description	Dimension	Tolerance ±
B01	Vertical CL of solder pad array (Datum G) to CL of (shell) solder pads	6.85	Basic
B02	Vertical CL of solder pad array (Datum G) to CL of outboard (right) locating hole	6.28	Basic
B03	Vertical CL of solder pad array (Datum G) to CL of inboard (left) locating hole	5.62	Basic
B04	CL of inboard locating hole to keep-out zone (length)	1.21	0.15
B05	Horizontal CL of solder pad array (Datum F) to CL of inboard (left) locating hole	0.95	Basic
B06	Connector keep-out zone height	4.32	0.15
B07	Horizontal CL of solder pad array (Datum F) to CL of small (left) solder pad	0.37	Basic
B08	Small (shell) solder pad height	1.40	0.10
B09	(Shell) solder pad width (2X)	1.90	0.10
B10	CL to CL of outer solder pads (horizontal)	10.50	Basic
B11	Vertical CL of solder pad array (Datum G) to CL outside solder pads	5.25	Basic
B12	Vertical CL of solder pad array (Datum G) to CL inside solder pads	4.75	Basic
B13	Signal solder pad length (42x)	1.40	0.05
B14	Signal solder pad width (42x)	0.31	0.05
B15	Solder pad pitch	0.50	Basic
B16	Horizontal CL of solder pad array (Datum F) to CL of large solder-pad	0.20	Basic
B17	Horizontal CL (Row A) to CL (Row B) solder pads	1.91	Basic
B18	Large (shell) solder pad height	1.80	0.15
B19	Horizontal CL of solder pad array (Datum F) to CL outboard (right) locating hole	1.31	Basic
B20	Locating hole diameter (2X)	1.00	0.05
B21	CL of inboard (left) locating hole to keep-out zone	2.68	0.15
B22	Connector keep-out zone length	16.60	0.15
B23	Datum F to CL of hole for left shell solder tail hole	0.31	Basic
B24	Datum G to CL of left and right shell solder tails	6.58	Basic
B25	Datum F to CL of right shell solder tail hole	0.19	Basic
B26	Diameter of plated thru holes for shell solder tails	1.30	0.10

4.3. x4 Fixed Host Board-side Right Angle Connector

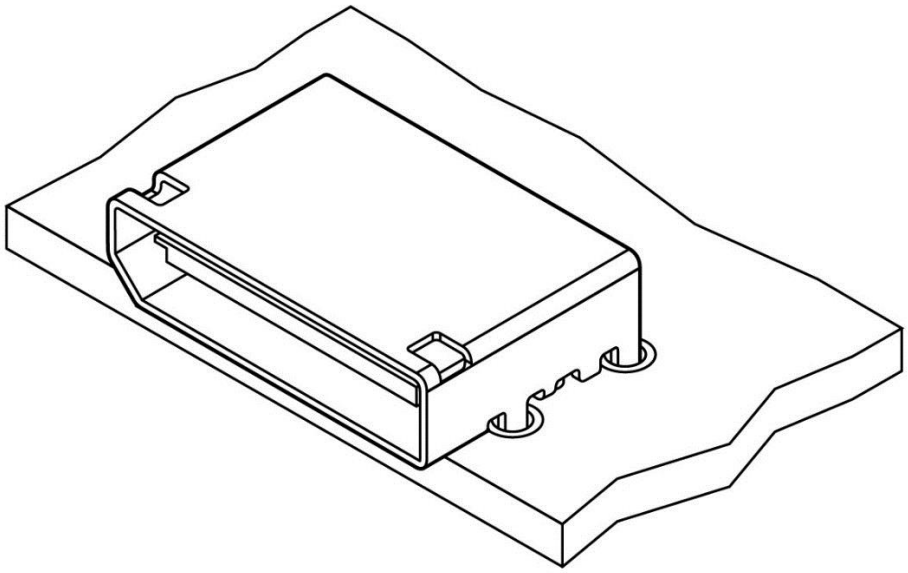


Figure 4-5. Isometric View of the x4 Fixed Host Board-side Right Angle Connector

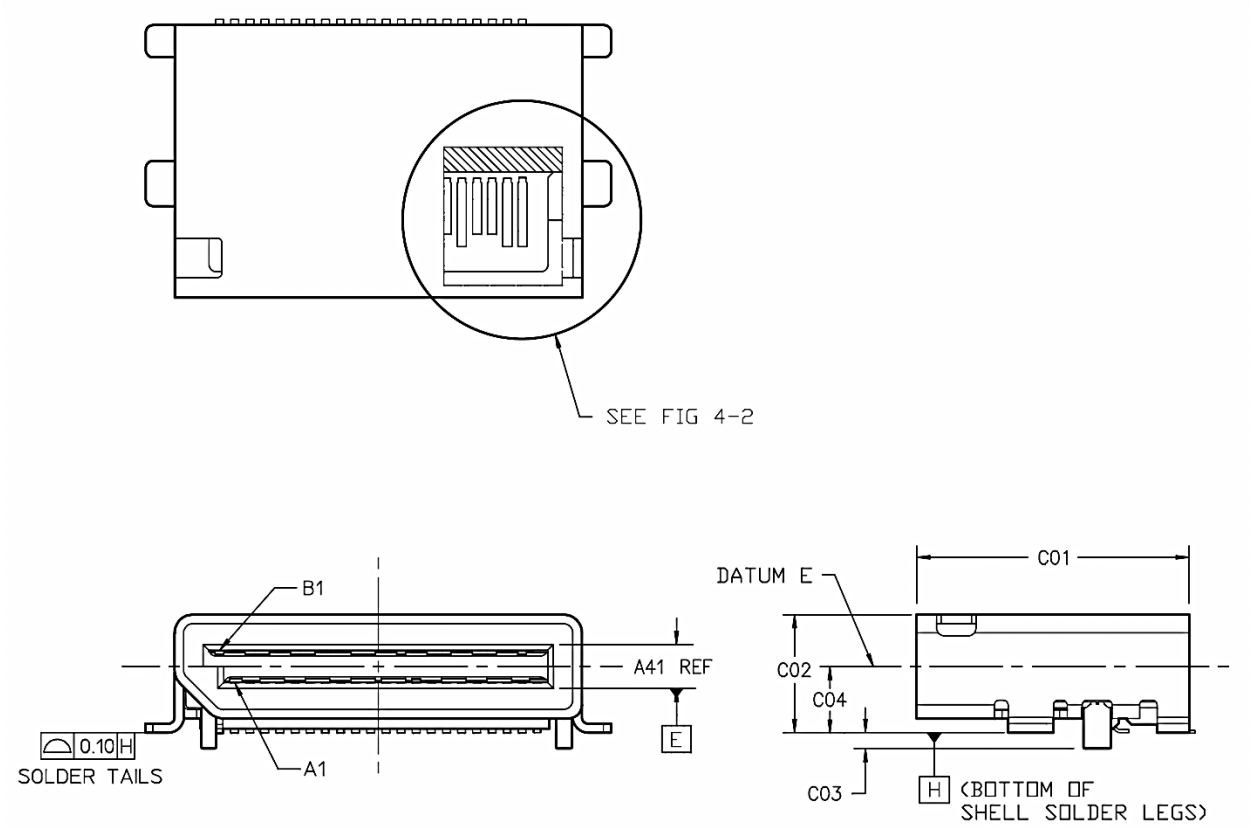


Figure 4-6. x4 Fixed Host Board-side Right Angle Connector Form Factor

Note: The x4 Fixed Host Board-side Right Angle Connector Mating Interface Dimensions are the same as for the Vertical version (see Figure 4-3).

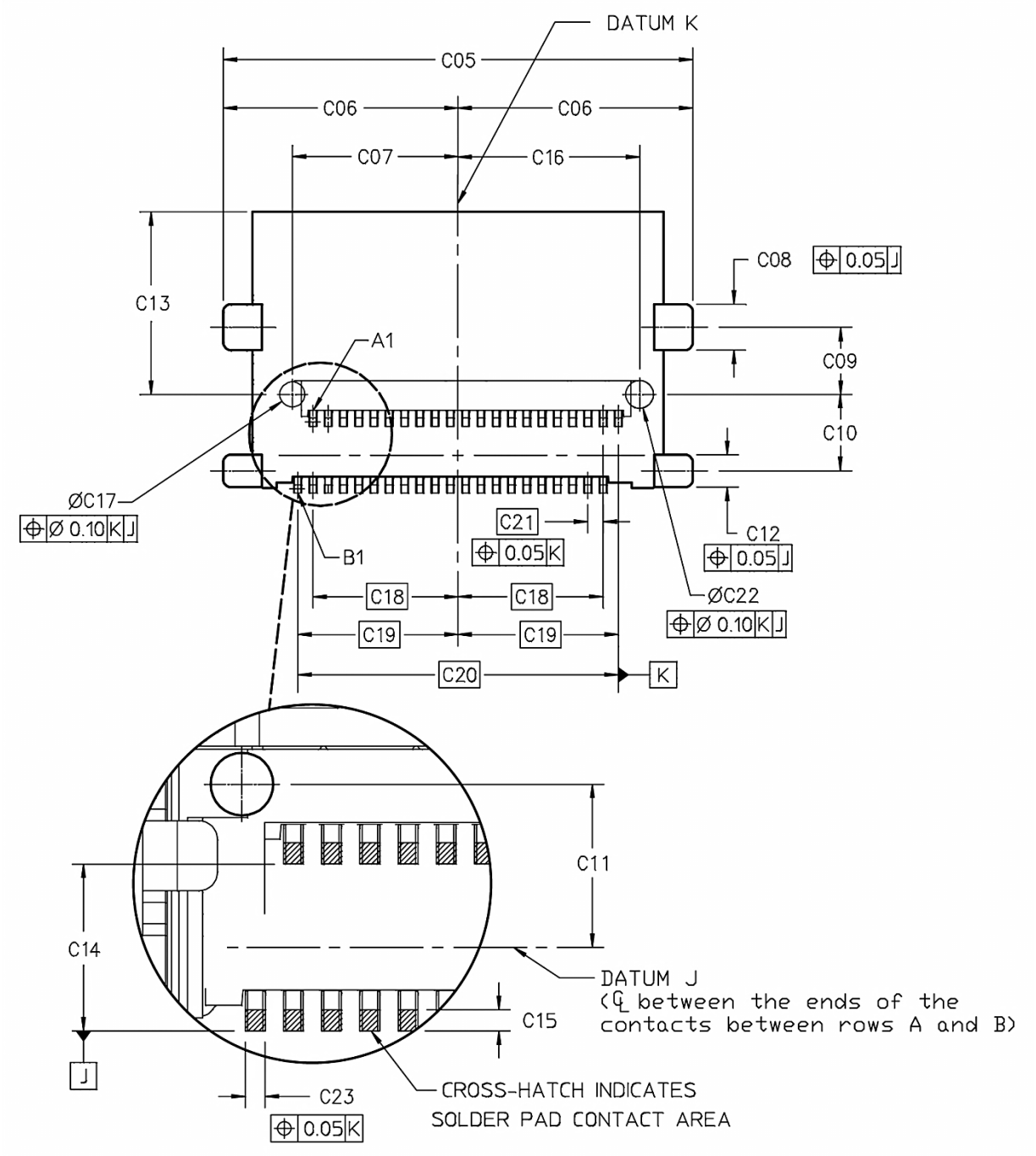


Figure 4-7. x4 Fixed Host Board-side Right Angle Connector Form Factor

Note: The x4 Fixed Host Board-side Right Angle Connector Mating Interface Dimensions are the same as for the Vertical version (see Figure 4-3).

Table 4-3. x4 Fixed Host Board-side Right Angle Connector Dimensions

ID	Description	Dimension	Tolerance ±
C01	Connector (shell) length	9.00	0.05
C02	Connector (shell) height from bottom of shell solder legs (Datum H)	3.90	Ref
C03	Locating peg length (2X)	0.52	0.10
C04	CL of interface paddle thickness (Datum E) to bottom of shell solder legs (Datum H)	2.19	0.08
C05	Length from end of left to end of right solder legs	15.38	0.10
C06	Vertical CL of solder tail array (Datum K) to outside edge solder leg (2X)	7.69	0.05
C07	Vertical CL of solder tail array (Datum K) to CL of left locating peg	5.42	0.08
C08	Large shell solder leg width	1.50	0.10
C09	Horizontal CL locating pegs to CL of large solder legs	2.20	0.11
C10	Horizontal CL locating pegs to CL of small solder leg	2.50	0.11
C11	Horizontal CL of locating pegs to CL solder tail array (Datum J)	2.14	0.19
C12	Small solder leg width	1.06	0.10
C13	Horizontal CL of locating pegs to front of shell	5.97	0.11
C14	End of solder tail Row “A” contacts to end of solder tail Row “B” contacts	2.18	0.16
C15	Length of solder pad contact area	0.28	0.03
C16	Vertical CL of solder tail array (Datum K) to CL of right locating peg	5.95	0.08
C17	Small (left) locating peg diameter	0.82	+0.03/-0.15
C18	Vertical CL of solder tail array (Datum K) to CL of inside solder tails	4.75	Basic
C19	Vertical CL of solder tail array (Datum K) to CL of outside solder tails	5.25	Basic
C20	CL to CL of outside solder tails	10.50	Basic
C21	Solder tail contact pitch	0.50	Basic
C22	Right locating peg diameter	0.97	+0.03/-0.15
C23	Solder tail width (solder pad contact area) (42x)	0.26	0.03

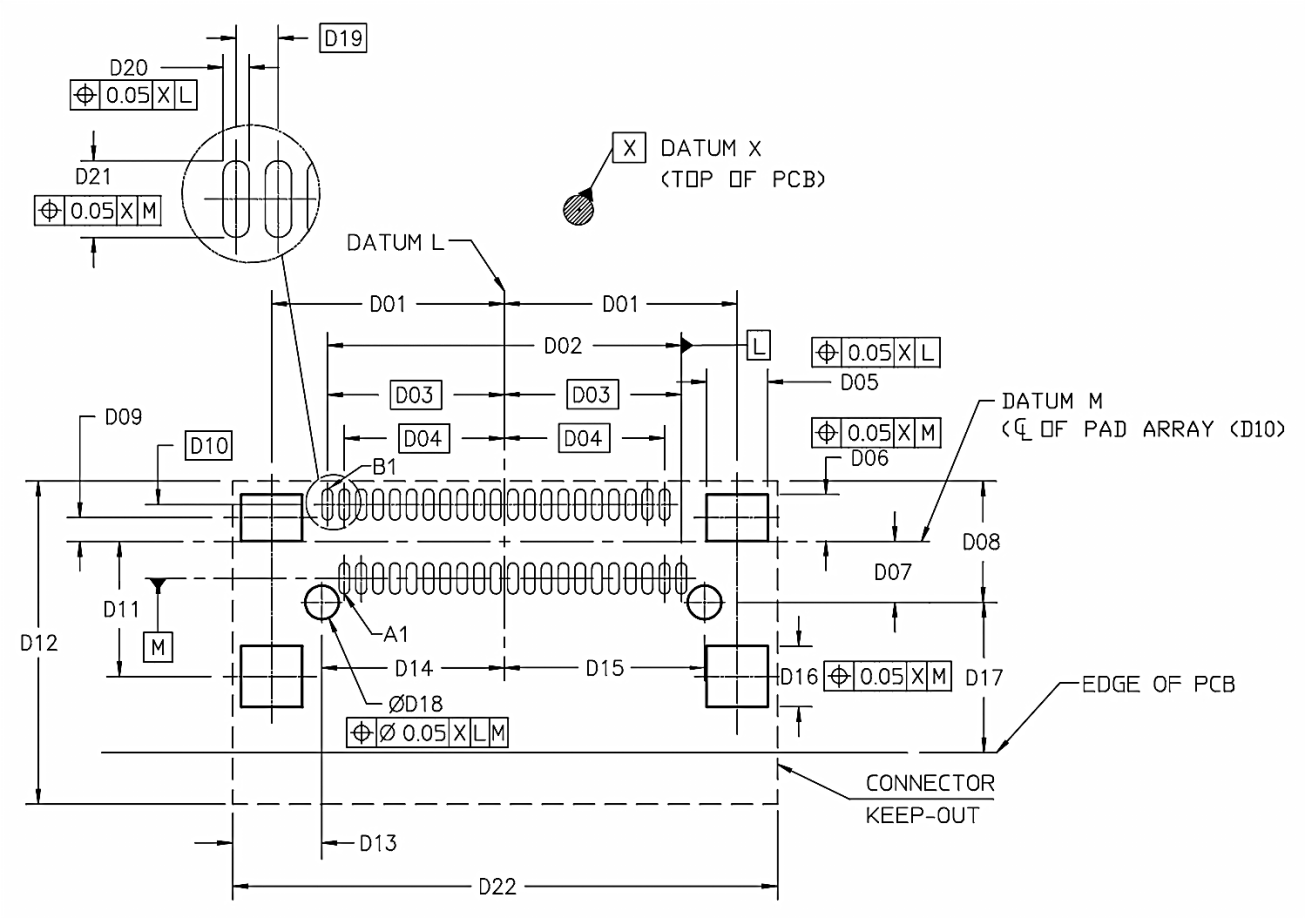


Figure 4-8. x4 Fixed Host Board-side Right Angle Connector Contact Footprint

Table 4-4. Fixed Host Board-side x4 Right Angle Connector Contact Footprint Dimensions

ID	Description	Dimension	Tolerance ±
D01	Vertical CL of solder pad array (Datum L) to CL shell solder pads (4X)	6.91	0.05
D02	Vertical CL to CL of outside shell solder pads	10.50	0.05
D03	Vertical CL of solder pad array (Datum L) to outside solder pads	5.25	Basic
D04	Vertical CL of solder pad array (Datum L) to inside solder pads	4.75	Basic
D05	Shell solder pad width (4X)	1.81	0.10
D06	Small shell solder pad length (2X)	1.38	0.10
D07	Horizontal CL of locating holes to CL of solder pad array (Datum M)	1.81	0.10
D08	CL locating holes to back keep-out	3.45	0.10
D09	Horizontal CL of solder pad array (Datum M) to CL of small shell solder pads (2X)	0.71	0.10
D10	Horizontal CL of row B solder pads to CL of row A Solder-Pads	2.19	Basic
D11	Horizontal CL of solder-Pad Array (Datum M) to CL of large shell solder pads (2X)	4.01	0.05
D12	Connector (shell) depth keep-out zone	10.42	0.15
D13	CL locating hole to left side of connector keep-out zone	6.47	0.15
D14	Vertical CL of solder pad array (Datum L) to CL left locating hole	5.41	0.05
D15	Vertical CL of solder pad array (Datum L) to CL right locating hole	5.94	0.05
D16	Large shell solder pad length (2X)	1.80	0.10
D17	Horizontal CL of locating holes to front edge of PCB	4.46	0.10
D18	Locating hole diameter (2X)	1.00	0.05
D19	Solder pad pitch	0.50	Basic
D20	Solder pad width (42x)	0.31	0.03
D21	Solder pad length (42x)	0.91	0.03
D22	Horizontal width of connector keep-out zone	17.25	0.15

4.4. x4 Fixed Host Board-side Connector Latching

- The windows in the top of the x4 Fixed Host Board-side right angle connector and the windows in the side wall of the Fixed (host-side) vertical connector serve as the latching points for the Free (Cable-side) latches (see Chapter 6).
- The windows accept both passive and active latching solutions that are defined on the Free Cable-side. The windows are located in relation to the connector contacts to enable the Cable-side to reliably mate to the host-side connector with acceptable minimum contact wipe in worst case tolerance conditions.
- As the x4 Fixed (Board-side) connectors are the same for both external and internal applications, the latch points are the same for both (see Figure 4-2).

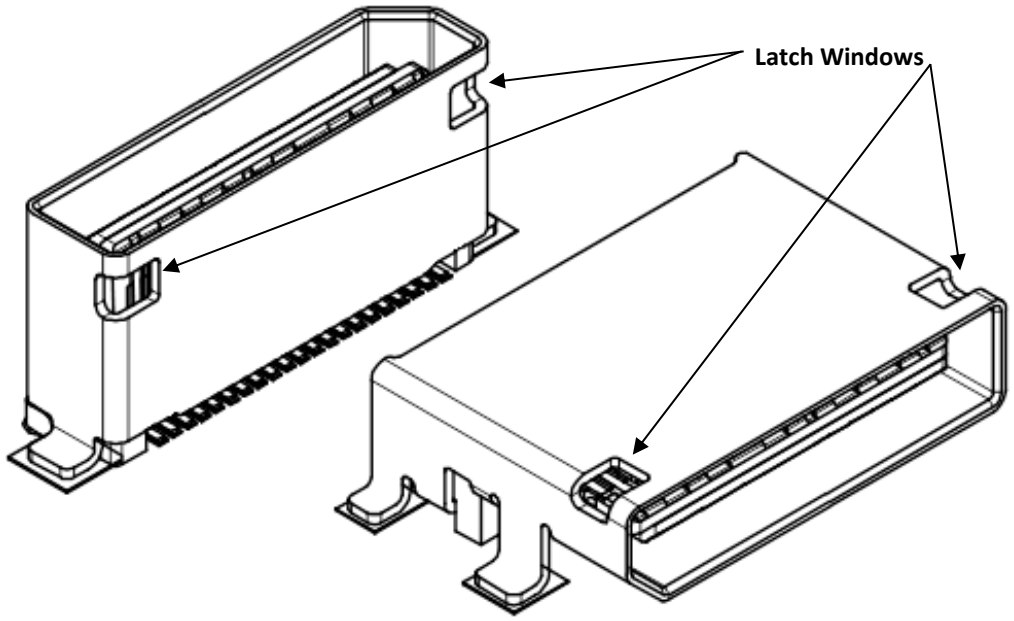


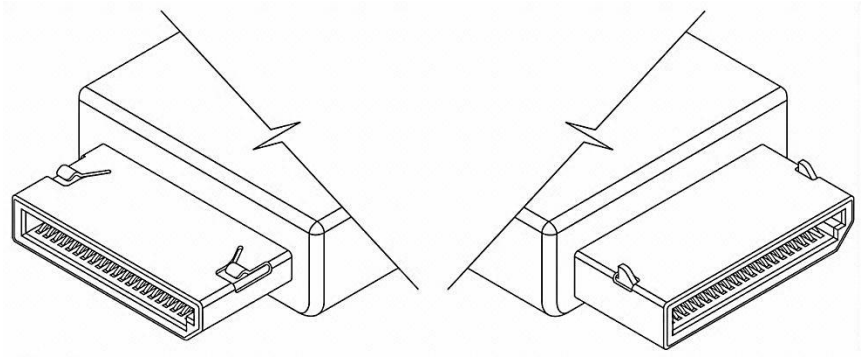
Figure 4-9. Isometrics of x4 Fixed Host Board-side Connectors with Latching Windows detail

5

5. x4 Free Cable side Connector

The x4 Free Cable-side Connector mates with all x4 Host Board-side connectors.

- It must be capable of incorporating either passive or active latching solutions for finished cable assemblies to be mechanically retained to the x4 Fixed-side connectors.
- The bulk cable to connector attachment varies by the type of bulk cable, as well as the variety of cable exit solutions, and is left to the cable assembly suppliers to define. Completed cable assemblies must comply with the cable exit form factor dimensions, defined in this Specification.



Representative Passive Latch

Representative Active Latch

Figure 5-1. Isometric of the x4 Free Cable-side Mating Interface for all Passive and Active Latch Cable Assemblies

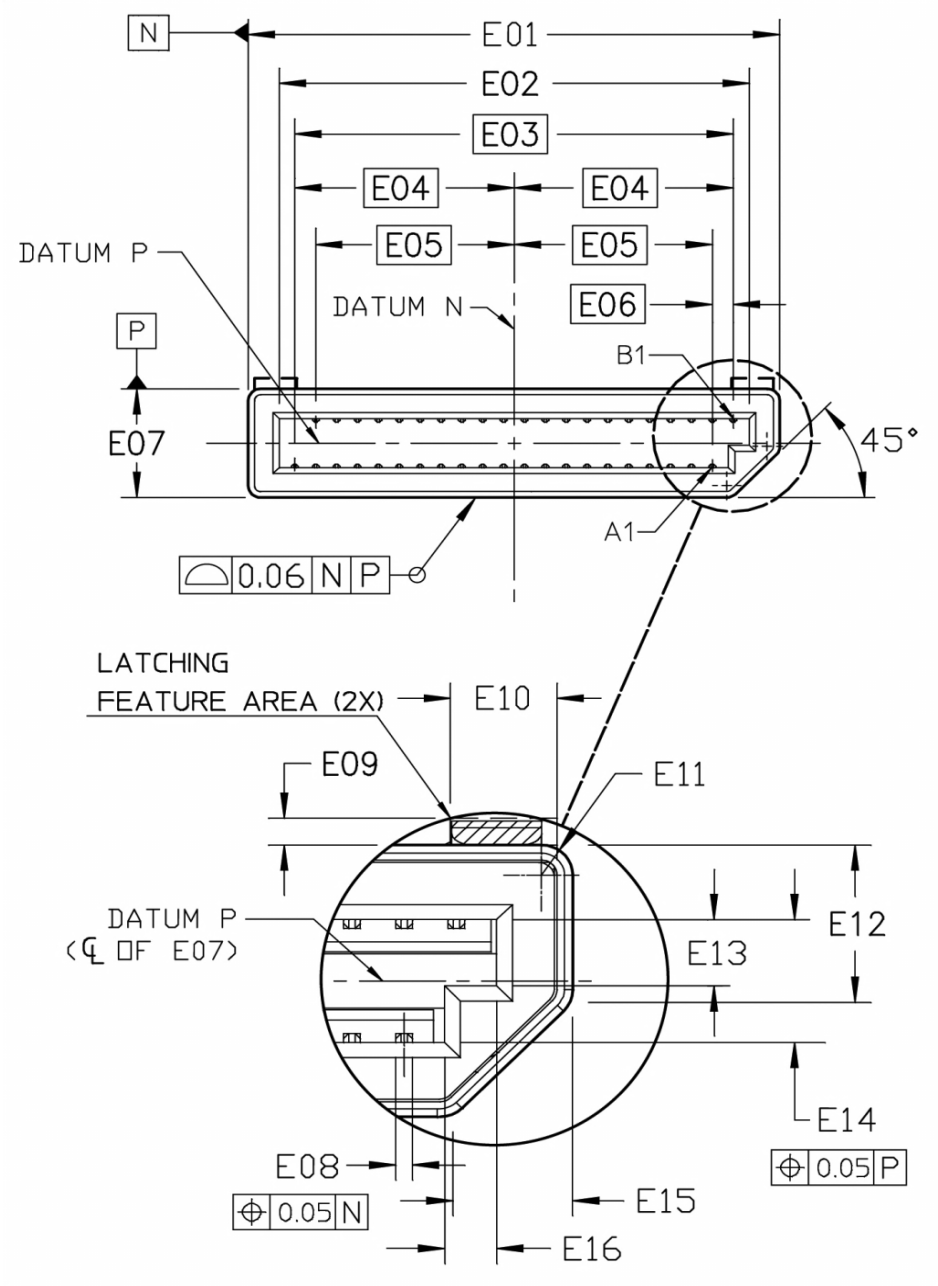


Figure 5-2. Mating Interface for x4 Free-side Cables

Dimensions apply to any Configuration Free-side Cable Interface.

Table 5-1. Dimensions for the x4 Free-side Cable Mating Interface

ID	Description	Dimension	Tolerance ±
E01	Connector Shell width (Datum N)	12.73	0.03
E02	Upper row interface width	11.28	0.03
E03	CL to CL of outside of contact beams	10.50	Basic
E04	Vertical CL of connector shell to CL outside contact beams	5.25	Basic
E05	Vertical CL of connector shell to CL of inside contact beams	4.75	Basic
E06	Contact beam pitch	0.50	Basic
E07	Connector shell height (Datum P)	2.72	0.03
E08	Contact beam width (42x)	0.16	0.03
E09	Clearance area reserved for latching mechanism (height) (2X)	0.43	0.05
E10	Clearance area reserved for latching mechanism (width) (2X)	1.05	0.05
E11	Outside radius (all)	0.30	MAX
E12	Top of shell to polarizing feature	1.57	0.04
E13	Polarizing notch height	0.67	0.03
E14	Interface cavity height (A side to B side)	1.23	0.05
E15	Side of shell to inside polarizing feature	1.15	0.05
E16	Polarizing notch width	0.50	Ref
E17	Interface width minus the polarizing feature	10.70	0.03

6

6. x4 Free Cable Assemblies

This chapter specifies x4 Free Cable Assembly attributes, signal pinouts and mechanical details, including drawings for the cable assembly form factors. The x4 Free internal cable assemblies have different constructions from the external box-to-box Free Cables and are shown separately.

6.1. x4 Free Cable Assembly Attributes

- Both passive and active cables must be invisible to system software (i.e., they are treated as software-transparent).
- Dual bundle, single bundle and ribbon cable solutions are acceptable, providing they meet all performance and form factor requirements (not all versions are shown).
- All x4 Free Cable Assemblies have the same pin numbering, as shown in Figure 6-1.
- See Table 3-1 and Table 3-2 for the Fixed internal connector pin assignments and Table 3-3 for the Fixed external connector pin assignments – *they are different*.

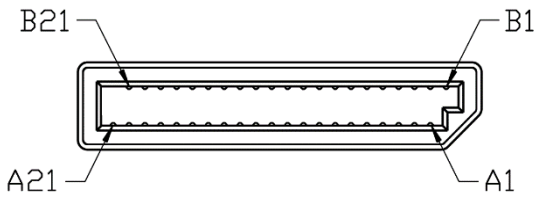


Figure 6-1. Pin number locations for x4 Free Cable Assemblies

6.1.1. x4 Passive Free Cable Solution Attributes

- Must not contain active components to (re-)drive the PCI Express signals across the cable.
- Is permitted to be limited to relatively short lengths; (i.e., 1 m – 2 m).
- Shielding may not be required for internal cables.

6.1.2. x4 Active Free Cable Assembly Attributes

- All external cable assemblies must provide 360° shielding from end to end.
- Is permitted to be implemented using copper or optical physical media.
- Is permitted to support maximum peripheral power of 10 W (equally distributed on the two 5 V power pins specified).
- Is permitted to support arbitrarily long cable lengths, as constrained by the active component power budget and PCI Express clocking schemes, in specific applications.
- Additional information regarding Active cables is contained in Appendix E.

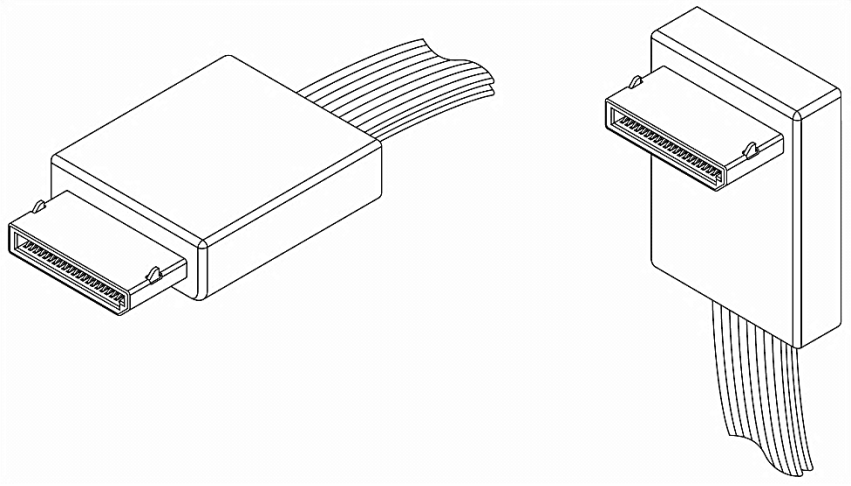
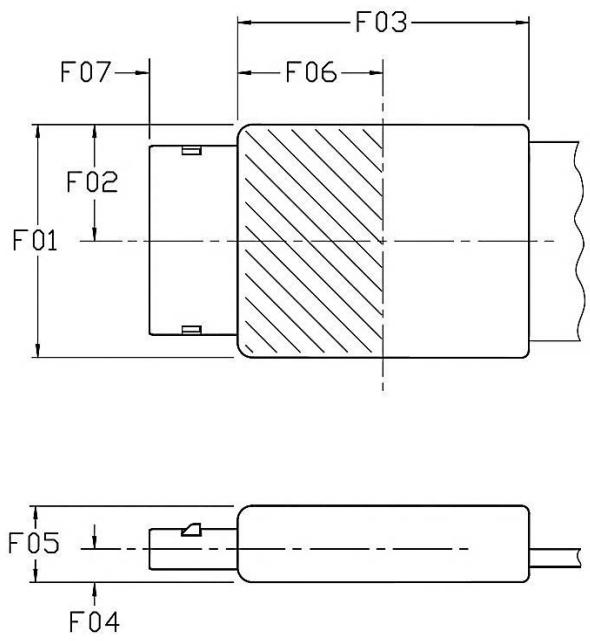


Figure 6-2. Isometrics of x4 Free Internal Straight-out Exit and Right Angle Exit Cable Assemblies

- See Chapter 5 for x4 Free Cable-side Connector mating interface dimensions.
- See Figure 6-9 and Figure 6-10for contact and latch locations for any Free-side cable interface.
- See Sections 4.1 and 4.2 for the x4 Fixed Host Board-side Vertical Connector dimensions.
- See Wiring Charts in Chapter 6 for cable assembly wiring.
- Ribbon cable shown for internal cables; other bulk cable solutions are acceptable for both external and internal solutions.

6.2. x4 Free Internal Cable Specification

6.2.1. x4 Free Internal Straight-out Cable Exit Assembly Form Factor



Note: Release Latch to keep within the cross-hatched area of F01 and F06.

Figure 6-3. x4 Free Internal Straight-out Cable Exit Form Factor

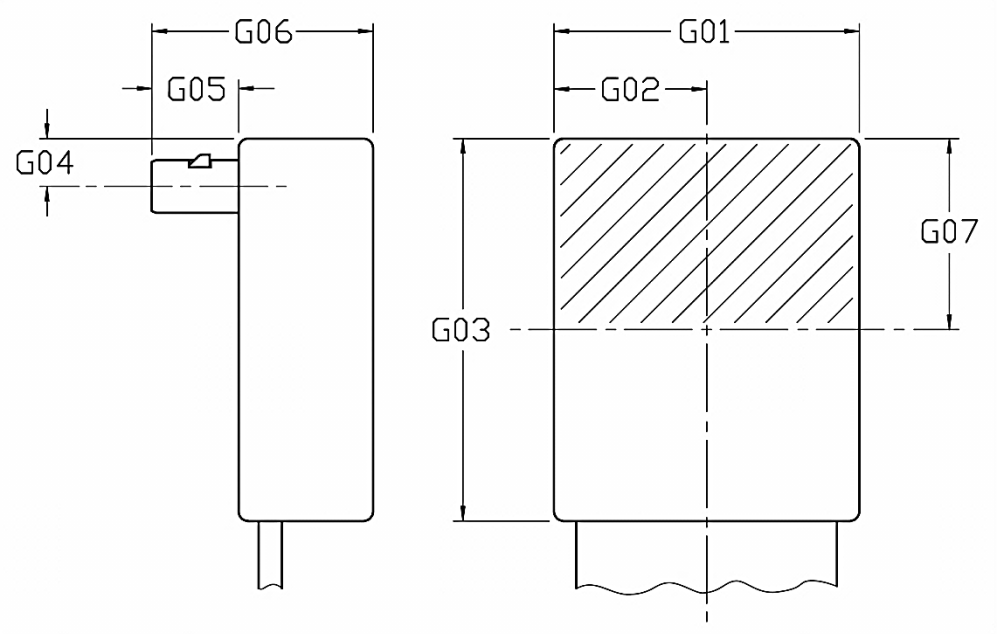
Table 6-1. Dimensions for x4 Free Internal Straight-out Cable Exit Form Factor

Designator	Description	Dimension	Tolerance ±
F01	Housing width	17.00	MAX
F02	CL to housing edge	As required for F01	
F03	Housing length	20.00	MAX
F04	Connector CL to bottom of housing	2.20 (Note 1)	MAX
F05	Housing thickness	7.25	MAX
F06	Boundary for release latch	10.1	MAX
F07	Connector snout length	5.95	0.25

Notes:1. Required to enable the plug to be mated to a Mid-board-mounted x4 Fixed Right Angle Connector.

2. See Figure 6-9 and Table 6-7 for passive latch dimensions.

6.2.2 x4 Free Internal Right-angle Down Cable Exit Assembly Form Factor



Note: Release Latch to keep within the cross-hatched area of G01 and G07

Figure 6-4. x4 Free Internal Right angle Down Cable Exit Form Factor

Table 6-2. Dimensions for x4 Free Internal Passive Right-Angle Down Cable Assembly Form Factor

Designator	Description	Dimension	Tolerance ±
G01	Housing width	17.00	MAX
G02	CL to housing edge	As Required by G01	
G03	Housing length	21.0	MAX
G04	Connector interface CL to edge of housing	6.5	MAX
G05	Connector snout length	5.0	MAX
G06	Overall height of plug	9.8 (Note 1)	MAX
G07	Boundary for release latch	10.1	MAX

Notes:

1. Enables mated height to remain below the maximum component height on a PCIe add-in card when mated to a x4 vertical host-side connector.
2. See Figure 6-8 and Table 6-10 for active latch dimensions.

6.2.3 x4 Free Internal Cable Assembly Physical and Mechanical Performance

- Strain relief not required, but cable assembly must meet application requirements.
- Additional mechanical requirements are stated in Chapter 5.

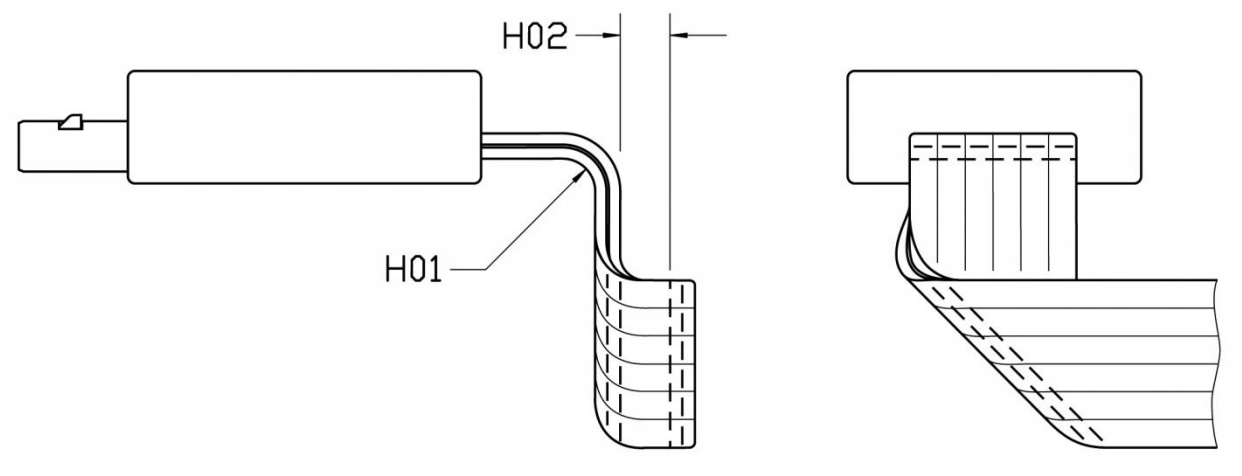


Figure 6-5. x4 Free Internal Cable Bend Radius

Table 6-3. x4 Free Internal Cable Flex Requirements

ID	Description	Dimension	Tolerance ±
H01	Cable Bend Radius	Bend R MIN supplier specific	Supplier specific
H02	Note: Flat cable must not be folded flat against itself when folded. A minimum clearance between cables at the fold must be supplier specific minimum to preserve the properties of the insulator and thereby the signal integrity.	MIN clearance for cable thickness fold radius supplier specific	

6.3. x4 Free External Passive Latch Cable Assembly Physical Form Factor

The physical form factor for the x4 Free External cable assembly is bounded by the dimensions shown in Figure 6-6 and Table 6-2.

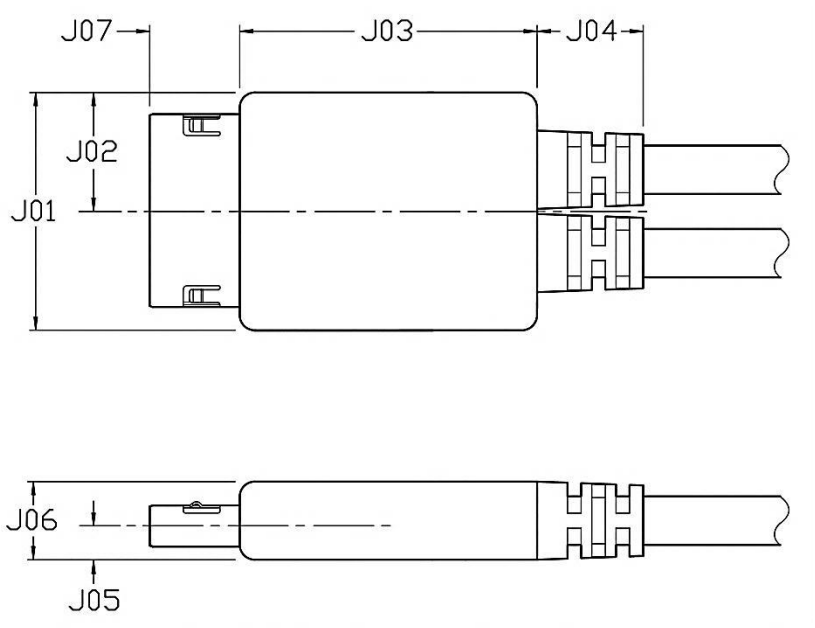


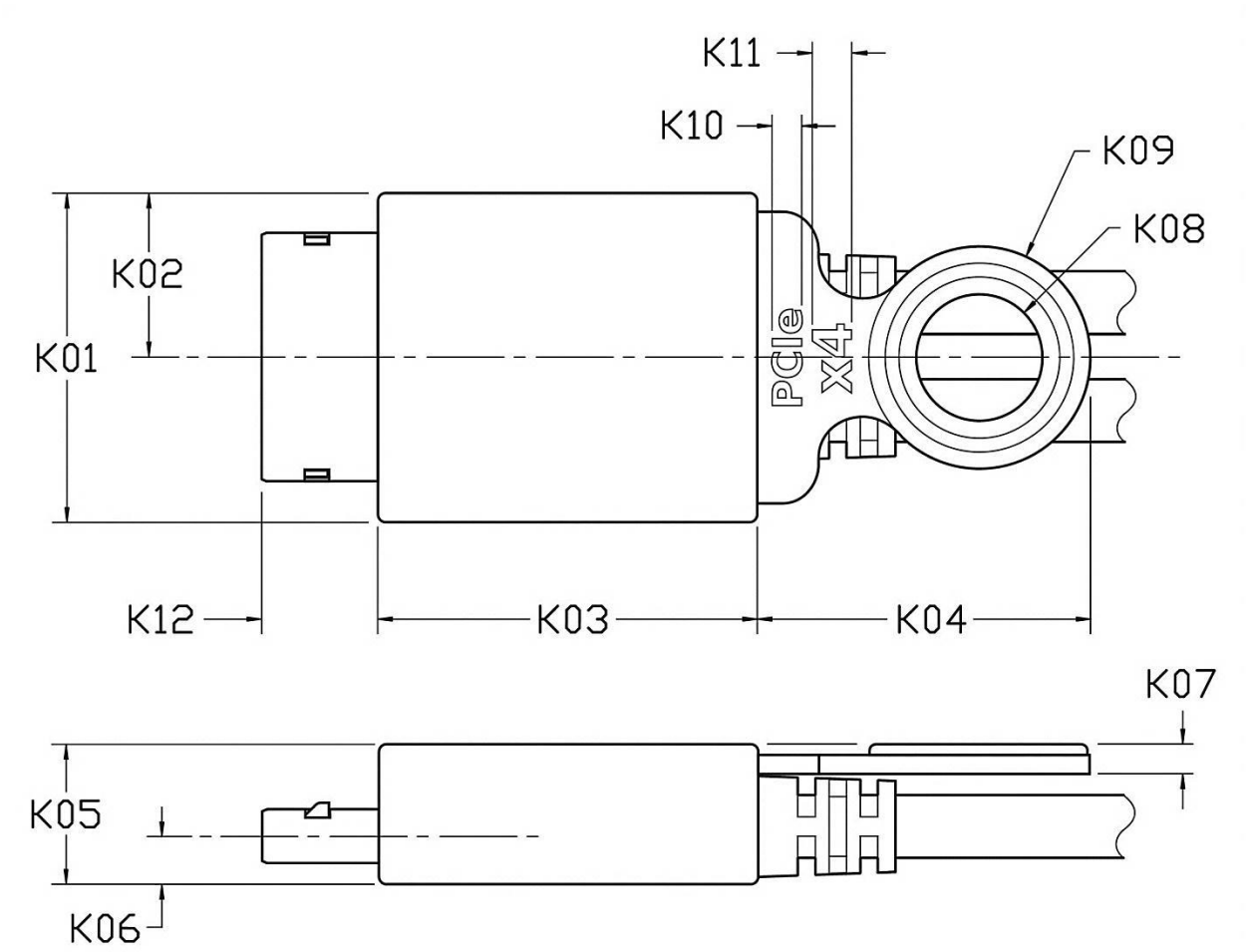
Figure 6-6. x4 Free External Passive Latch Cable Assembly Form Factor Dimensions

Table 6-4. Dimensions for the x4 Free Passive Latch External Cable Assembly Form Factor

Designator	Description	Dimension	Tolerance ±
J01	Width of housing	17.00	MAX
J02	CL of housing to edge	As required for J01	
J03	Housing length	25.00	MAX
J04	Length of flex relief (optional)	7.75	MAX
J05	Connector CL to bottom of housing	2.60 (Note 1)	MAX
J06	Thickness of housing	7.25	MAX
J07	Connector snout length	5.95	0.25

Notes:
1. Enables belly-to-belly implementations on a 1.4 mm MIN thick host board.
2. See Figure 6-9 and Table 6-7 for passive latch dimensions.

6.4. x4 Free External Active Latch Cable Assembly Physical Form Factor



Note: PCI Express latch pull tab to be Pantone 354U Green

Figure 6-7. x4 Free External Active Latch Cable Assembly Form Factor Dimensions

Table 6-5. Dimensions for the x4 Free External Active Latch Cable Assembly Form Factor

ID	Description	Dimension	Tolerance ±
K01	Width of housing	17.00	MAX
K02	Connector CL to edge of housing	As required for K01	
K03	Length of housing	25.00	MAX
K04	Pull tab length	20.00	MAX
K05	Thickness of housing	7.25	MAX
K06	CL of shell interface to bottom of housing	2.60 (Note 1)	MAX
K07	Pull tab thickness	1.5	MAX
K08	Diameter of opening in pull tab	6.4	0.5
K09	Outer radius of pull tab	5.7	0.5
K10	Height of PCIe characters	1.5	0.15
K11	Height of the x4 characters	2.0	0.15
K12	Connector snout length	5.95	0.25

Notes:
1. Enables belly-to-belly implementations on a 1.57 mm MIN thick host board.
2. See Figure 6-10 and Table 6-8 for active latch dimensions.

6.5. x4 Free External Cable Assembly Physical and Mechanical Performance

- Table 6-6 lists the external cable bend radius requirements for static bending.
- Additional mechanical requirements are stated in Section 6.9

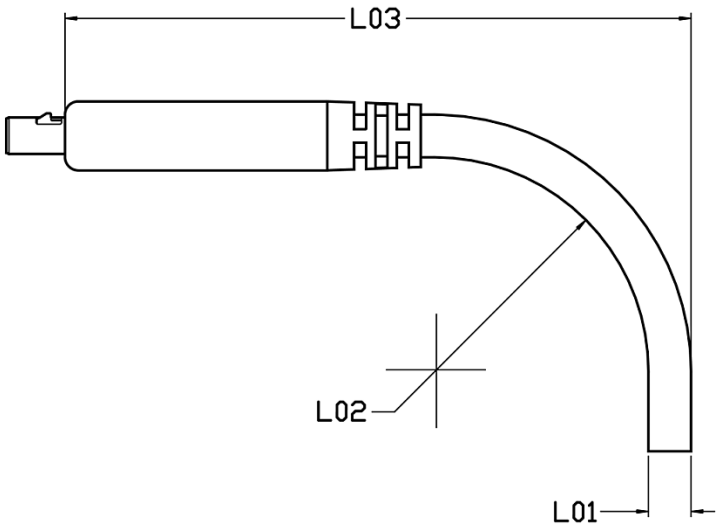


Figure 6-8. x4 Free External Cable Assembly Bend Radius

Table 6-6. x4 Free External Cable Assembly Bend Radius Requirements

Designator	Description	Dimension	Tolerance ±
L01	34 AWG 4-pair cable diameter	Supplier specific	Supplier specific
L02	Inner bend radius	Supplier specific by gage	MIN
L03	Face of connector housing to outside of cable bend	42.80	3.0

6.6. Latching for All x4 Free Cable Assemblies

Figure 6-9 and Figure 6-10 show representative latch configurations. Specific shapes are left to the cable supplier, but must meet the insertion force and latch retention forces, defined in this Specification, when mated with and latched to the windows defined in the Fixed-side connectors, defined in this Specification.

See Figure 5-2 for the maximum allowable latch protrusion above the Fixed-side shell.

6.6.1. Passive Latching for All x4 Free Cable Assemblies

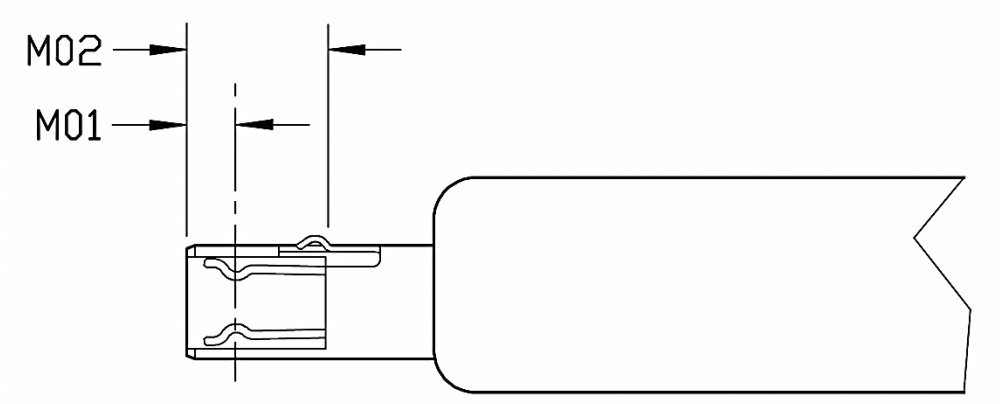


Figure 6-9. Passive Latching Dimensions for x4 Free Cable Assemblies

Table 6-7. Dimensions for the x4 Free Cable Passive Latch

ID	Description	Dimension	Tolerance ±
M01	Front of connector to contact point	1.19	0.11
M02	Front of connector to passive latch retention point	3.49	0.20

6.6.2. Active Latching for All x4 Free Cable Assemblies

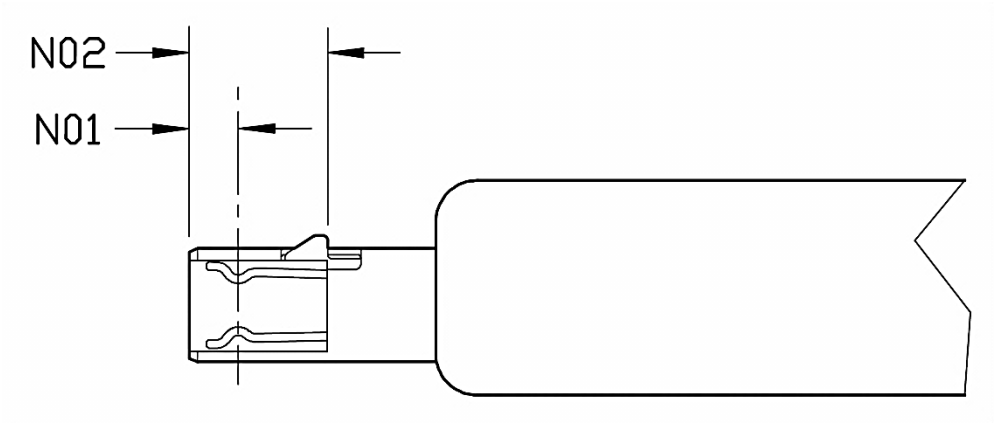


Figure 6-10. Active Latching Dimensions for x4 Free Cable Assemblies

Table 6-8. Dimensions for the x4 Free Active Cable Active Latch

ID	Description	Dimension	Tolerance ±
N01	Front of connector to contact point of terminal	1.19	0.11
N02	Front of connector to active latch retention point	3.34	0.14

6.7. Free Cable Assembly Wiring Charts

- All Internal ribbon cables are to be wired as complete crossovers.
- Internal unassigned pins to be wired to enable crossover functionality
- Internal and External cable assemblies are not interchangeable.
- External 5 V power does not crossover

6.7.1. Wiring Chart for Internal Cables

- See Internal Connector Pinout Table 3-1 and Table 3-2.
- The wiring charts for Passive and Active cable assemblies are the same.
- Active cables are defined as having active components only within the cable plug.
- The Fixed side must provide the 3.3 V to support an optional active cable.

Table 6-9. Wiring Chart for Internal Passive and Active Crossover Cables

	Row	ROOT/ Downstream	Cable Termination & Signal Direction	Row	END POINT/ Upstream
1	A1	POWER 3.3 Vact RX	NO WIRE	B1	RESERVED
2	A2	GROUND	———	B2	GROUND
3	A3	PERp0	← ———	B3	PETp0
4	A4	PERn0	← ———	B4	PETn0
5	A5	GROUND	———	B5	GROUND
6	A6	PERp1	← ———	B6	PETp1
7	A7	PERn1	← ———	B7	PETn1
8	A8	GROUND	———	B8	GROUND
9	A9	BP TYPE	← ———	B9	BP TYPE
10	A10	CWAKE# (Note 1)	← ———	B10	CWAKE#
11	A11	GROUND	———	B11	GROUND
12	A12	VSP	———	B12	VSP
13	A13	VSP	———	B13	VSP
14	A14	GROUND	———	B14	GROUND
15	A15	PERp2	← ———	B15	PETp2
16	A16	PERn2	← ———	B16	PETn2
17	A17	GROUND	———	B17	GROUND
18	A18	PERp3	← ———	B18	PETp3
19	A19	PERn3	← ———	B19	PETn3
20	A20	GROUND	———	B20	GROUND
21	A21	RESERVED	NO WIRE	B21	POWER 3.3 Vact TX

Note:

1. CWAKE# is permitted to also be used for OBFF and if both ends support OBFF the signal becomes bidirectional.

Table 6-9. (Cont'd). Wiring Chart for Internal Passive and Active Crossover Cables.

	Row	ROOT/ Downstream	Cable Termination & Signal Direction	Row	END POINT/ Upstream
1	B1	RESERVED	NO WIRE	A1	POWER 3.3 Vact RX
2	B2	GROUND	———	A2	GROUND
3	B3	PETp0	——→	A3	PERp0
4	B4	PETn0	——→	A4	PERn0
5	B5	GROUND	———	A5	GROUND
6	B6	PETp1	——→	A6	PERp1
7	B7	PETn1	——→	A7	PERn1
8	B8	GROUND	———	A8	GROUND
9	B9	2-WIRE CLOCK	←——→	A9	2-WIRE CLOCK
10	B10	2-WIRE DATA	←——→	A10	2-WIRE DATA
11	B11	GROUND	———	A11	GROUND
12	B12	PERST#	——→	A12	PERST#
13	B13	CPRSNT#	←——	A13	CPRSNT#
14	B14	GROUND	———	A14	GROUND
15	B15	PETp2	——→	A15	PERp2
16	B16	PETn2	——→	A16	PERn2
17	B17	GROUND	———	A17	GROUND
18	B18	PETp3	——→	A18	PERp3
19	B19	PETn3	——→	A19	PERn3
20	B20	GROUND	———	A20	GROUND
21	B21	POWER 3.3 Vact TX	NO WIRE	A21	RESERVED

6.7.2. Wiring Chart for External Cables

- See External Connector Pinout Table 3-3.
- This is not a full crossover cable, only the high speed lines crossover.
- The wiring charts for Passive and Active cable assemblies are the same.
- Active cables are defined as having active components only within the cable plug.
- The Fixed side must provide the 3.3 V to support an optional active cable.
- The Fixed side must provide the 5 V for Optional Power.

Table 6-10. Wiring Chart for External Passive and Active Cables; with and without Power

	Row	ROOT/ Downstream	Cable Termination & Signal Direction	Row	END POINT/ Upstream
1	A1	POWER 3.3 Vact RX	NO WIRE	A1	POWER 3.3 Vact RX
2	A2	GROUND	———	B2	GROUND
3	A3	PERp0	←	B3	PETp0
4	A4	PERn0	←	B4	PETn0
5	A5	GROUND	———	B5	GROUND
6	A6	PERp1	←	B6	PETp1
7	A7	PERn1	←	B7	PETn1
8	A8	GROUND	———	B8	GROUND
9	A9	UNASSIGNED	———	A9	UNASSIGNED
10	A10	CWAKE# (Note 1)	←	A10	CWAKE#
11	A11	GROUND	———	B11	GROUND
12	A12	VSP	———	A12	VSP
13	A13	VSP	———	A13	VSP
14	A14	GROUND	———	B14	GROUND
15	A15	PERp2	←	B15	PETp2
16	A16	PERn2	←	B16	PETn2
17	A17	GROUND	———	B17	GROUND
18	A18	PERp3	←	B18	PETp3
19	A19	PERn3	←	B19	PETn3
20	A20	GROUND	———	B20	GROUND
21	A21	POWER 5 V #2	AS REQUIRED	A21	POWER 5 V #2

Note:

1. CWAKE# is permitied to also be used for OBFF and if both ends support OBFF the signal becomes bidirectional.

Table 6-10 (Cont'd). Wiring Chart for External Passive and Active Crossover Cables, with and without Power

	Row	ROOT/ Downstream	Cable Termination & Signal Direction	Row	END POINT/ Upstream
1	B1	POWER 5 V #1	AS REQUIRED	B1	POWER 5 V #1
2	B2	GROUND	———	A2	GROUND
3	B3	PETp0	——→	A3	PERp0
4	B4	PETn0	——→	A4	PERn0
5	B5	GROUND	———	A5	GROUND
6	B6	PETp1	——→	A6	PERp1
7	B7	PETn1	——→	A7	PERn1
8	B8	GROUND	———	A8	GROUND
9	B9	2-WIRE CLOCK	AS REQUIRED	B9	2-WIRE CLOCK
10	B10	2-WIRE DATA	AS REQUIRED	B10	2-WIRE DATA
11	B11	GROUND	———	A11	GROUND
12	B12	PERST#	——→	B12	PERST#
13	B13	CPRSNT#	←——	B13	CPRSNT#
14	B14	GROUND	———	A14	GROUND
15	B15	PETp2	——→	A15	PERp2
16	B16	PETn2	——→	A16	PERn2
17	B17	GROUND	———	A17	GROUND
18	B18	PETp3	——→	A18	PERp3
19	B19	PETn3	——→	A19	PERn3
20	B20	GROUND	———	A20	GROUND
21	B21	POWER 3.3 Vact TX	NO WIRE	B21	POWER 3.3 Vact TX

6.8. Memory Map

The management interface memory map of PCI Express OCuLink cables is defined in detail in Appendix A.

6.9. Performance Requirements for Connectors and Cables

This Specification conforms to the test sequences, as defined in *EIA 364 TS-1000*. It is recommended that the OCuLink Fixed (Board-side) and Free (Cable-side) connectors to be used in PCI Express Subsystems be tested in accordance with *EIA 364.1000-01*, using the appropriate test sequences.

6.9.1. Current and Voltage Requirements

The current and voltage requirements are defined in *ANSI/EIA-364-70*.

Table 6-11. Connector Electrical Requirements

Description	Requirement	Procedure
Contact Continuous Current Carrying Capability	All contacts 0.5 A per contact MAX. - **except** - The two 5 V pins to be 1 A per contact MAX.	30 **°C maximum temperature rise**
Voltage	30 VDC per contact	
Low Level Contact Resistance	Baseline	20 mVDC, 10 mA *EIA 364-23*
Insulation Resistance (Note 1)	100 MΩ minimum between adjacent contacts (unmated).	100 VDC
Dielectric Withstanding Voltage (Note 1)	No defect or breakdown between adjacent contacts.	250 VDC minimum for 100 ms

Notes:

1. The minimum Hi-Pot requirement for cable assemblies is determined by the Insulation Resistance and the Dielectric withstanding Voltage.

Table 6-12. Connector Environmental Requirements

Description	Requirement
Field Life	3 years
Field Operating Temperature - External	-25 °C ~ +55 °C
Field Operating Temperature - Internal	-25 °C ~ +60 °C
Test Group 4 Option	1B
Storage Temperature	-40 °C to +85 °C
Storage Humidity	80 % Relative Humidity

Table 6-13. Connector Mechanical Requirements

Description	Requirement	Procedure
Contact Interface Plating Type	Noble	
Surface Treatment (Lubricated or non-Lubricated)	Specified by Manufacturer	
Rated Durability Cycles – External	10,000	
Rated Durability Cycles – Internal	50	
Vibration	No Damage. No discontinuity longer than 1 microsecond allowed. 30 mΩ maximum change from initial (baseline) contact resistance.	*EIA 364-28* Condition III
Mechanical Shock	No Damage. No discontinuity longer than one microsecond allowed. 30 mΩ maximum change from initial (baseline) contact resistance.	*EIA 364-27* Condition A

Table 6-14. Connector/Cable Latching Requirements

Description	Min	Max	Units	Conditions / Comments
Mating Force				Rate 19-31 mm/s *EIA 364-13*
- Connector (w/out latch)	2	20	N	
- Connector W/ Passive Latch	10	40	N	
- Connector W/Active Latch	8	40	N	
Un-Mating Force				Rate 19-31 mm/s *EIA 364-13*
- Connector (w/out latch)	1	16	N	
- Connector W/ Passive Latch	8	25	N	
- Connector W/Active Latch W/Pull	8	25	N	
Wrenching Strength W/ Mated Cable- Passive Latch		25	N	Bend cable 90 degrees at minimum bend radius. Pull in 4 axis directions for round cable. Pull in 2 axis directions for flat cable. No damage to plug/cable assembly.
Wrenching Strength W/ Mated Cable- Active Latch		40	N	Bend cable 90 degrees at minimum bend radius. Pull in 4 axis directions for round cable. Pull in 2 axis directions for flat cable. No damage to plug/cable assembly.
Active Latch Retention Strength	30		N	No damage to plug/cable assembly below Minimum Value

7

7. Electrical Topologies and Link Definitions

7.1. Electrical Topologies and Link Definitions

This section defines the electrical characteristics for the cable assembly. This Specification ensures successful communication between the PCI Express signal input and output Links at the system host board. The cable Specification includes the cable assembly and the mating host board connectors.

Unless otherwise noted, the Specifications contained herein apply to all high-speed signals defined for each interface width. The signaling rate for encoded data is 8.0 GT/s. The signaling is point-to-point and requirements are only defined for 8.0 GT/s.

The 5.0 GT/s and 2.5 GT/s signaling rates are outside the scope of this Specification. Their specifications can be found in *PCI Express Base Specification,* Rev. 2.0 and Rev. 1.1, respectively.

7.1.1. Topologies

Possible electrical topologies for the OCuLink PCI Express form factor are:

- Internal connector/cable assembly
  Examples would be: system board to mid-plane, add-in Card to system board
- External connector/cable assembly (shown on a Low profile add-in Card)
  Examples would be: system board to external device, system board 1 to system board 2

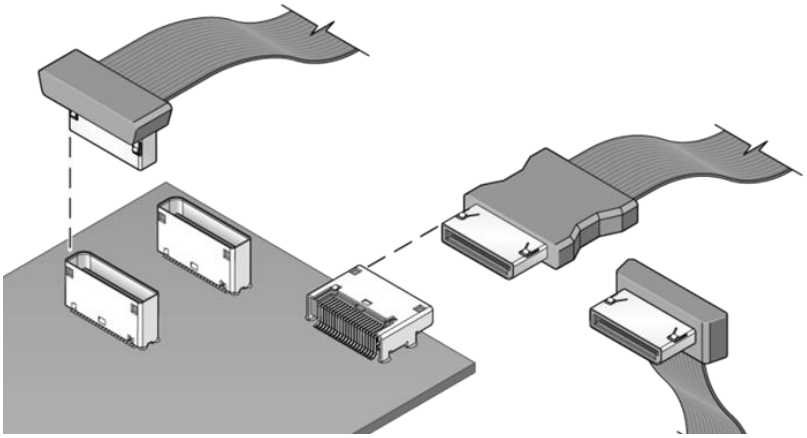


Figure 7-1. Representative OCuLink Internal Topologies

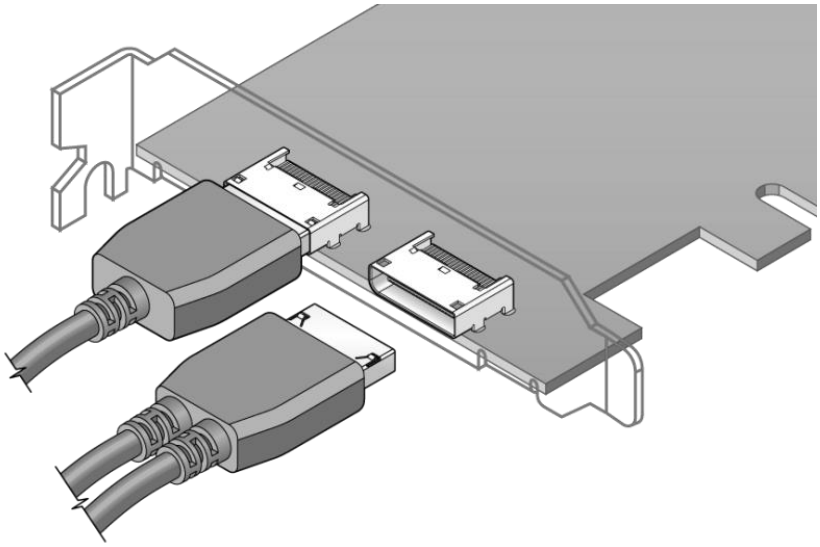


Figure 7-2. Representative OCuLink External Topology

7.1.2. Link Definitions

Typical OCuLink form factor components (as shown in Figure 7-3) consist of the following:

- OCuLink Fixed Host-side PCB Connector
- OCuLink Free Cable Assembly with Free Connectors
- OCuLink Fixed Host-side PCB Connector

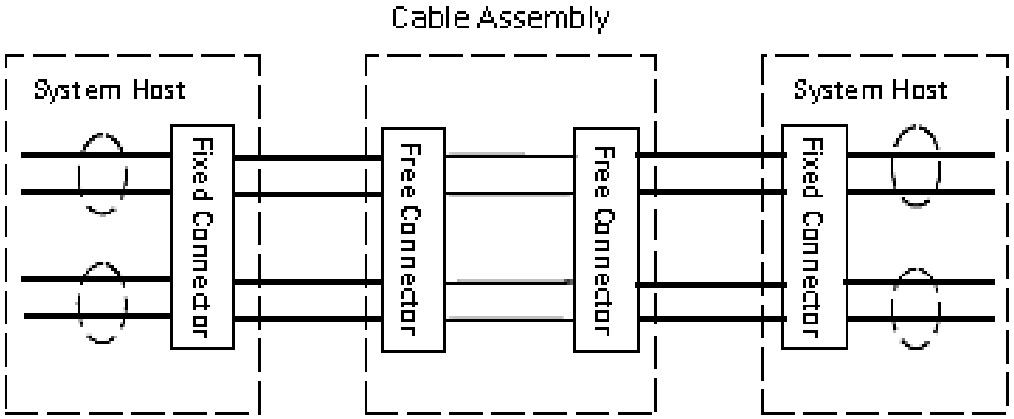


Figure 7-3. Connector/Cable Diagram

7.2. Link Measurement Points

The electrical measurement points for the cable are shown in Figure 7-4. The measurements are made using Cable Compliance Boards (CCBs). The effects of the CCBs are removed/de-embedded from the measurement using a TRL method (see Section 7.4).

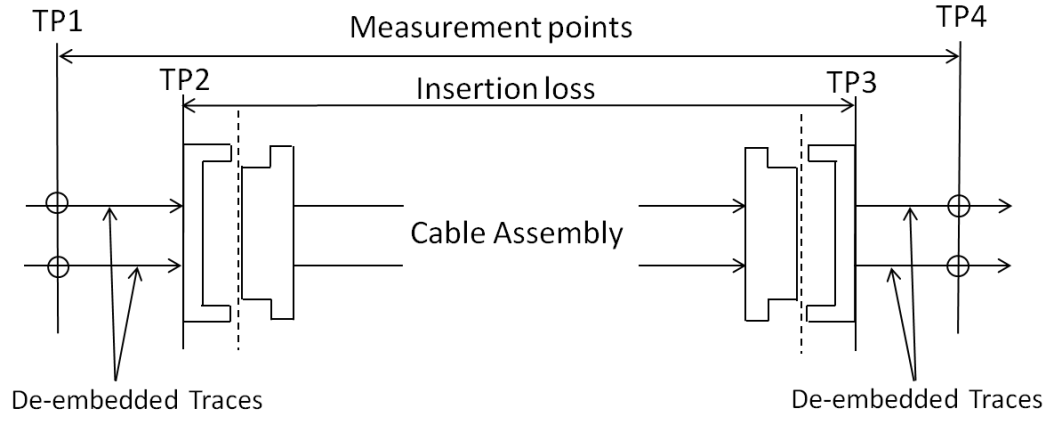


Figure 7-4: Cable Assembly Measurement Points

7.3. Cable Electrical Specifications

The OCuLink cable assembly contains insulated conductors terminated in a connector at each end for use as a Link segment between host boards. This cable assembly is primarily intended as a point-to-point interface between host boards using controlled impedance cables. All cable assembly measurements are to be made between TP1 and TP4 with CCB test fixtures. These cable assembly Specifications are based upon twin axial cable characteristics. Table 7-1 provides a summary of the cable assembly characteristics and references addressing each parameter. Reported values are at 4 GHz. Note that plots show loss (positive values).

Table 7-1. Cable Assembly Differential Characteristics Summary

Description	Reference	Value	Unit
Maximum insertion loss	7.3.2	15	dB
Minimum insertion loss	7.3.2	0	dB
Minimum return loss	7.3.3	Equation (7-5)	dB
Differential to common-mode return loss	7.3.4	Equation (7-6)	dB
Differential to common-mode conversion loss minus Insertion Loss	7.3.5	Equation (7-7)	dB
Common-mode to common-mode return loss	7.3.6	Equation (7-8)	dB
MDNEXT loss	7.3.7	Equation (7-9)	dB
MDFEXT loss	7.3.7	Equation (7-10)	dB
OCuLink Total Cable Assembly Skew (Sc)	7.3.8	6	ns MAX

7.3.1. Characteristic Impedance and Reference Impedance

The nominal differential characteristic impedance of the cable assembly is 85 Ω. The differential reference impedance for cable assembly Specifications must be 85 Ω.

7.3.2. Pinout for x4 Fixed Internal Connector (root)

The fitted cable assembly insertion loss *IL Cable fitted* (*f*), as a function of frequency *f*, is defined in Equation (7-1).

Equation (7-1)

$$\boldsymbol{ILCablefitted(f) = a_1\sqrt{f} + a_2 f + a_4 f^2}$$

Where:

	f	is the frequency in GHz
	ILCable(f)	is the fitted cable assembly insertion loss, in dB

Given the cable assembly insertion loss measured between TP1 and TP4 is at *N* uniformly-spaced frequencies f_n spanning the frequency range 50 MHz to 12000 MHz with a maximum frequency spacing of 10 MHz, the coefficients of the fitted insertion loss are determined using Equation (7-2) and Equation (7-3).

Define the frequency matrix, *F*, as shown in Equation (7-2).

Equation (7-2)

$$F = \begin{bmatrix} \sqrt{f_1} & f_1 & f_1^2 \\ \sqrt{f_2} & f_2 & f_2^2 \\ \cdots & \cdots & \cdots \\ \sqrt{f_N} & f_N & f_N^2 \end{bmatrix}$$

Note: The polynomial coefficients a_1, a_2 and a_4 are determined using Equation (7-3). In Equation (7-3), T denotes the matrix transpose operator and IL is a column vector of the measured insertion loss value, IL_n at each frequency, f_n.

Equation (7-3)

$$\begin{bmatrix} a_1 \\ a_2 \\ a_4 \end{bmatrix} = (F^T F)^{-1} F^T IL$$

Examples of maximum and minimum fitted insertion loss are illustrated in Figure 7-5. The coefficients for the maximum loss curve are: a1 = 6.9, a2 = 0.6, and a4 = 0.05.

The coefficients for the minimum loss curve are: a1 = 0.5, a2 = 0.18, and a4 = 0.

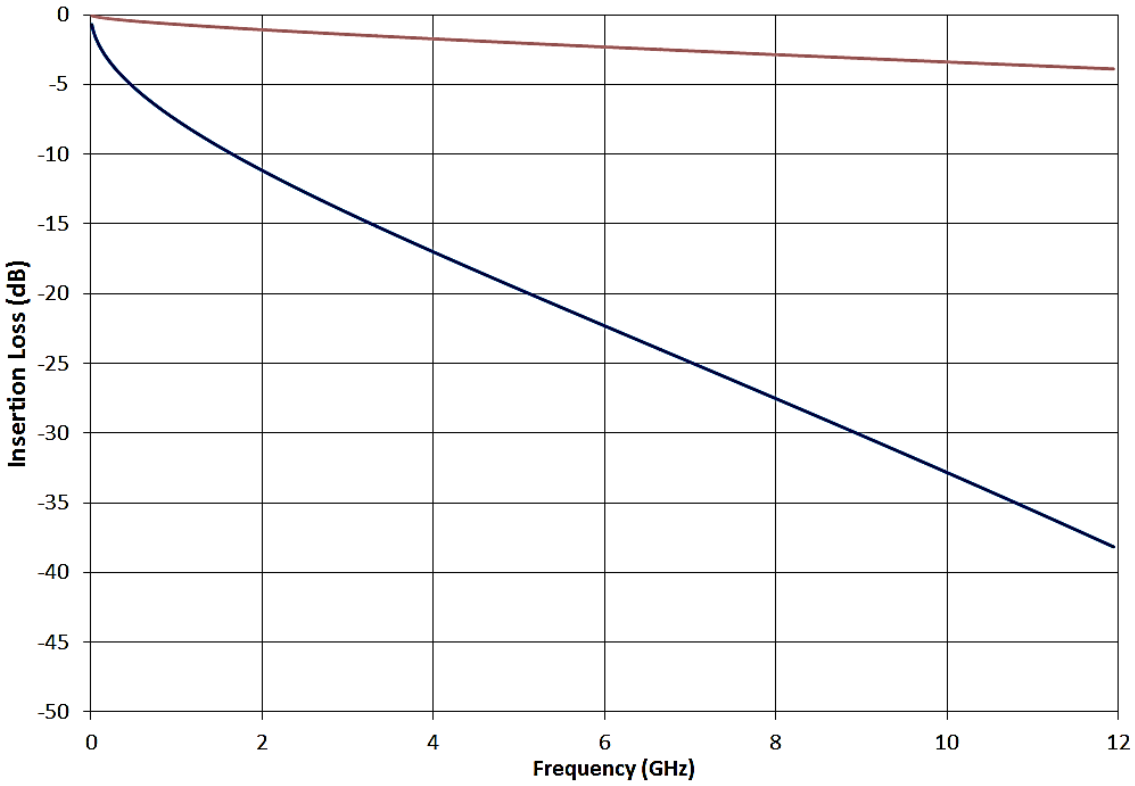


Figure 7-5: Example Cable Assembly Insertion Loss

7.3.3. Cable Assembly Differential Return Loss

The differential return loss of each pair of the OCuLink cable assembly must meet the values determined using Equation (7-4), as illustrated in Figure 7-6.

Equation (7-4)

$$RLCable(f) = \begin{cases} -10 \text{ dB for } 0.05 < f < 2 \text{ GHz} \\ (f\text{-}12) \text{ dB for } 2 < f < 8 \text{ GHz} \\ -4 \text{ dB for } 8 < f < 12 \text{ GHz} \end{cases}$$

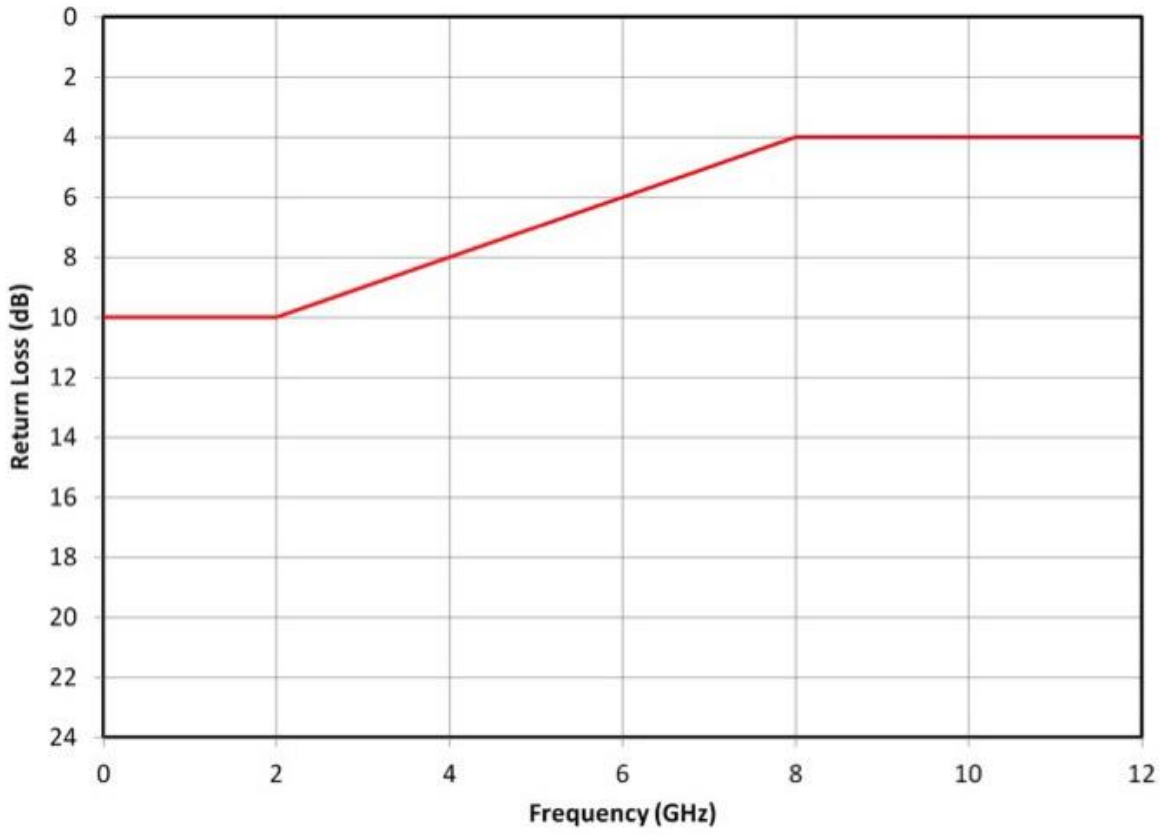


Figure 7-6: Minimum Cable Assembly Return Loss

7.3.4. Differential to common-mode return loss

The differential to common-mode return loss, in dB, of the cable assembly must meet Equation (7-5), as illustrated in Figure 7-7.

Equation (7-5)

$$\text{DifftoCMRLCable}(f) = (2/3)f - 20 \text{ dB for } 0.05 \text{ GHz} < f < 12 \text{ GHz}$$

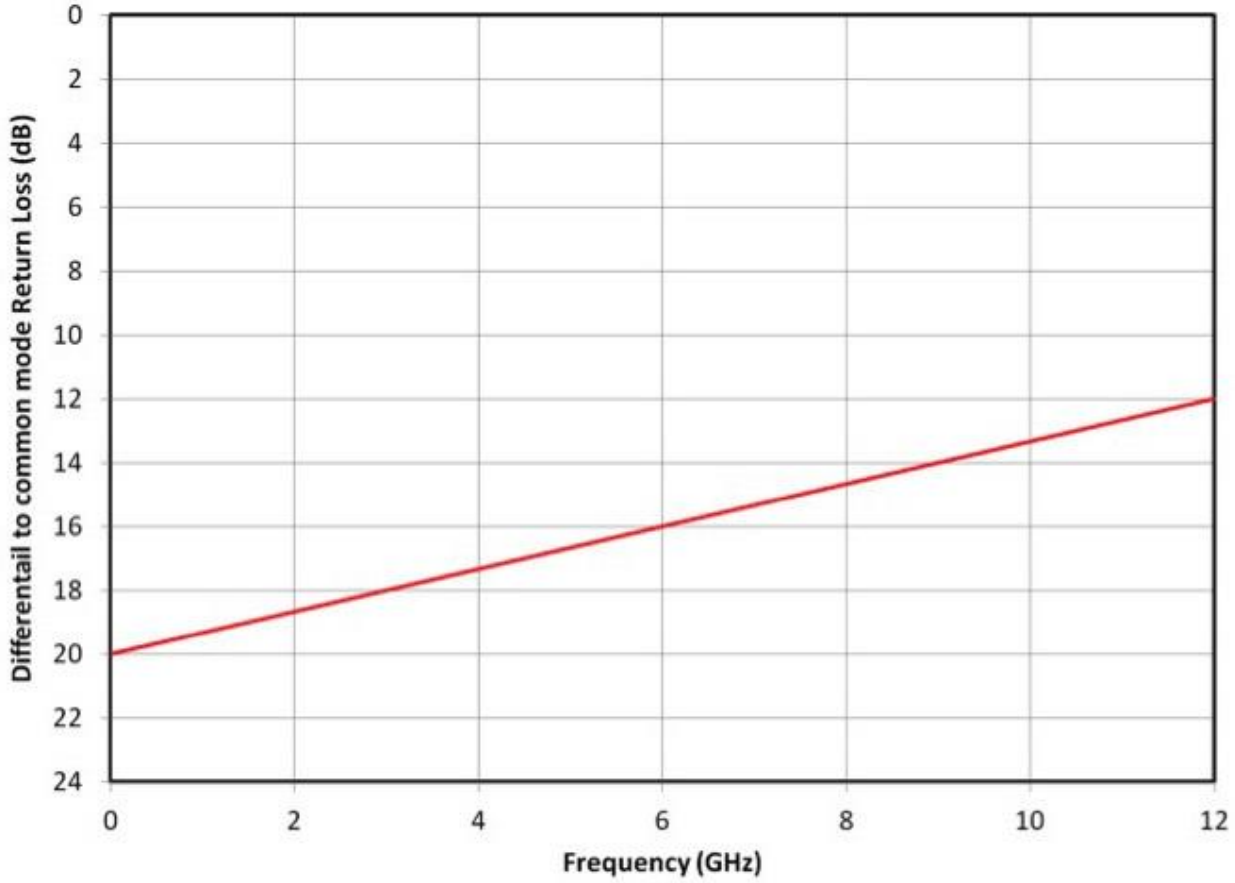


Figure 7-7: Differential to Common-mode Cable Assembly Return Loss

7.3.5. Differential to Common-mode Conversion Loss minus Insertion Loss

The difference between the cable assembly differential to common-mode conversion loss and the cable assembly insertion loss must meet Equation (7-6).

Equation (7-6)

$$\text{DifftoCMConv-IL}_{\text{Cable}}(f) = \quad -10 \text{ dB for } 0.05 < f < 12 \text{ GHz}$$

7.3.6. Common-mode to Common-mode Return Loss

The common-mode to common-mode return loss, in dB, of the cable assembly must meet Equation (7-7).

Equation (7-7)

$$\text{Cable}(f) = -2 \text{ dB for } 0.05 < f < 12 \text{ GHz}$$

7.3.7. Connector/Cable Crosstalk

All system board and cable assembly designs must properly account for any crosstalk that may exist among the various pairs of differential signals. Crosstalk may be either near-end (NEXT) or far-end (FEXT). Each component potentially, has impact on a design and must be planned for accordingly. The equation for NEXT is shown in Equation 7-8; the equation for FEXT is shown in Equation 7-9.

Crosstalk between differential pairs influences and impacts the data signals and any subsequent loss and jitter budgets. Note that all eye diagrams must account for any and all crosstalk present, in order to limit crosstalk impacts and implications. All system boards interfacing with a cable assembly must also properly account for crosstalk. The system board must also account for potential crosstalk that occurs on the printed circuit board, as well as within the connector itself.

Equation (7-8)

$$\mathbf{MDNEXT\_loss}(\boldsymbol{f}) = -\mathbf{10}\,\mathbf{log_{10}}\sum_{\boldsymbol{i=0}}^{\boldsymbol{i=3}}\mathbf{10}^{-\boldsymbol{NLi}(\boldsymbol{f})/\mathbf{10}} \quad \text{for 0.05 GHz} \leq f \leq \text{12 GHz}$$

Where:

MDNEXT_loss(*f*) is the MDNEXT loss at frequency *f*

$NL_i(f)$ is the NEXT loss at frequency *f* of pair combination i, in dB

F is the frequency, in GHz

i is the 0 to 3 (pair-to-pair combination)

The MDNEXT loss between a receive Lane and all transmit Lanes (e.g., closest in proximity) must meet the limits specified by Equation (7-9).

Equation 7-9)

$$\text{MDNEXT\_loss(f)} \geq 31.5 - 12.5 \times \log(f / 4)\ \text{dB} \qquad 0.05\ \text{GHz} \leq f \leq 12\ \text{GHz}$$

Where:

f is the frequency, in GHz

Equation (7-10)

$$\mathbf{MDFEXT\_loss}(\boldsymbol{f}) = -\mathbf{10}\,\mathbf{log_{10}}\sum_{\boldsymbol{i=0}}^{\boldsymbol{i=2}}\mathbf{10}^{-\boldsymbol{NLi}(\boldsymbol{f})/\mathbf{10}} \quad \text{for 0.05 GHz} \leq f \leq \text{12 GHz}$$

Where:

MDFEXT_loss(*f*) is the Multi-Disturber Far End Cross Talk loss at frequency *f*

$NL_i(f)$ is the FEXT loss at frequency *f* of pair combination i, in dB

F is the frequency, in GHz

i is the 0 to 2 (pair-to-pair combination)

The MDFEXT loss between a receive Lane at the far end and with the noise source (Transmitters) at the near end must meet the limits specified by Equation (7-11).

Equation (7-11)

$$MDFEXT\_loss(f) \geq 31 - 15 \times \log(f / 4)\ dB \qquad 0.05\ GHz \leq f \leq 12\ GHz$$

Where:

f is the frequency, in GHz

7.3.8. Connector/Cable Lane-to-Lane Skew

The skew at any point is measured using zero crossings of differential voltage of the compliance pattern, while simultaneously transmitting on all physical Lanes. The compliance pattern is defined in the *PCI Express Base Specification*.

7.4. TRL Cable Compliance Board (CCB) Trace De-embedding.

Utilizing test fixtures, cable compliance measurements are made at TP1 and TP4, as shown in Figure 7-8. The effects of the test fixtures are de-embedded, using the TRL method described in Section 7.4.1.

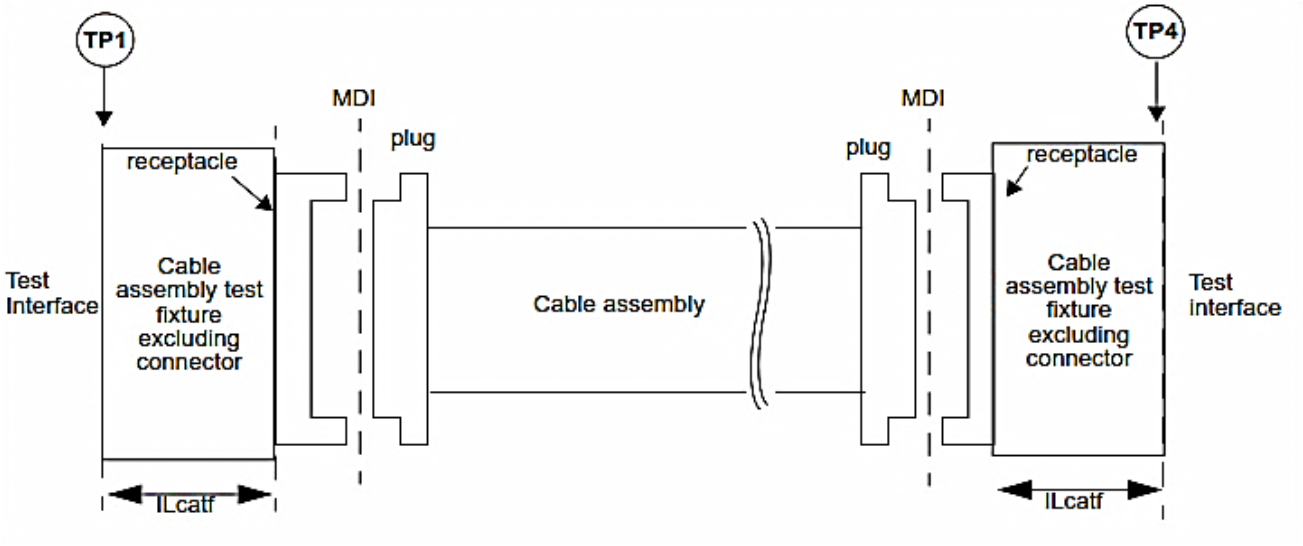


Figure 7-8. Cable Compliance Boards used in TRL calibration

7.4.1. CCB TRL Traces

The effects of the CCB on the measured cable s-parameters are removed using a Through, Reflect, Line (TRL) de-embedding technique. TRL has the advantage that it is able to be easily tailored to impedances other than 50 Ω. It is recommended that the OCuLink cable be measured in an 85 Ω environment, using single ended, micro-strip lines built to 42.5 Ω impedance. The TRL calibration kit, containing seven (7) calibration lines, is shown in Figure 7-9.

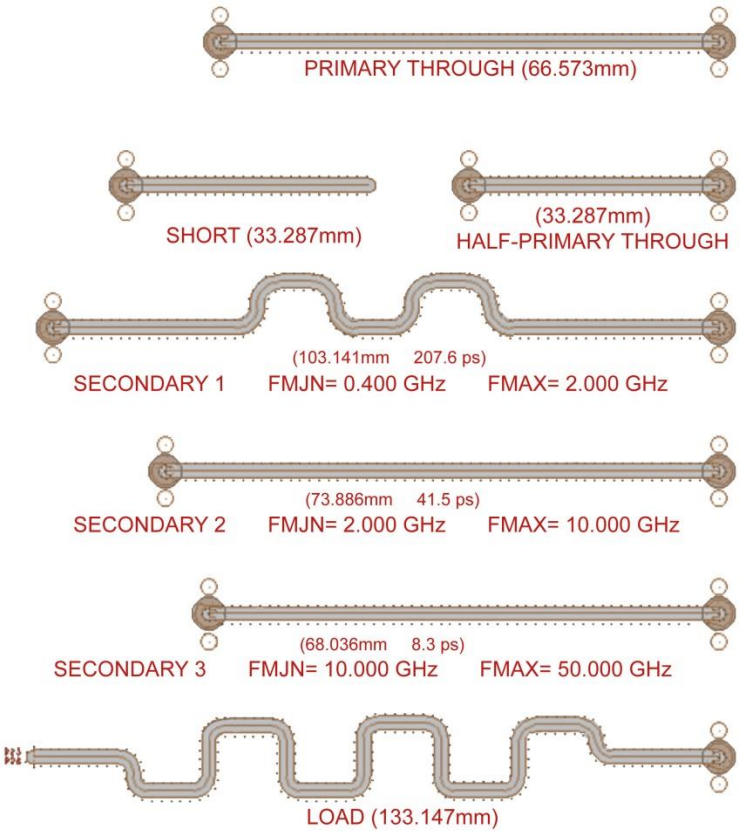


Figure 7-9 TRL Calibration Kit, used with MEG-6 stack-up, showing Primary Through, Half-Primary Through (L1), Secondary 1, Secondary 2, Secondary 3 and Load

7.4.2. Cable Compliance Board Through Line

The first calibration element consists of a transmission line that is exactly twice the length of the distance from each test port to the reference plane (L1). It is referred to as the “primary through” line. All lines on the board are designed to 42.5 Ω impedance. The Through and the Secondary lines establish the reference impedance for the measurement after calibration is completed. The network analyzer must be set to 42.5 Ω. Select Line Z0 on the network analyzer to ensure the analyzer uses the 42.5 Ω impedance of the line standard during measurement. Some tools mis-handle s-parameters with reference impedances other than 50 Ω. Check that the tool correctly recognizes the reference impedance used in the measurement.

7.4.3. Cable Compliance Board Reflect Line

The second calibration element consists of a transmission line that is exactly half the length of the primary through. The reflect standard is used to establish the position of the measurement reference plane.

7.4.4. Cable Compliance Secondary Lines

Secondary lines are used to extend the useful calibration frequency range. These added elements differ from the primary through only in their length. Secondary lines are required to not be integer multiples of half wavelengths. The total length of each secondary consists of the length of the primary through plus the added length calculated by the TRL secondary calculator. Secondary lines are built to match the impedance of the primary through and so establish the measurement impedance environment.

7.4.5. Cable Compliance Load Line

A structure consisting of a resistive load that matches the desired reference impedance is used to cover the lowest frequencies. Two 0201 size resistors in parallel make a termination useful from 10 MHz to 400 MHz.

7.4.6. Building TRL Lines

Building TRL lines requires tight control of trace impedance. Typically all traces are controlled to 42.5 Ω ± 2.25 Ω, single-ended impedance. The two boards used to test an individual cable assembly should be fabricated in the same PCB panel. It is recommended that the traces between the launch connector and the DUT be matched to within ±0.0127 mm. Launch connectors and the launch connector land pattern should be optimized to support at least 25 GHz. Avoid silkscreen over traces. Maintain 1.778 mm pitch between launch connectors. Use fiber weave mitigation design techniques with artwork rotation ≥ 7°. Build the TRL calibration as an inseparable structure on one of the two boards used to measure the cable under test.

7.4.7. Calculating TRL Secondary Line Lengths

The structures required to correctly de-embed the CCB test fixtures are able to be designed using a TRL calculator. The TRL calculator requires f_{min}, phase margin greater than 20° and effective Dk as inputs. The calculator outputs frequency range, trace length and delay time. The C-based source code is shown in Figure 7-4.

Figure 7-10 shows TRL Line Length Calculator Source Code for the calculations in TRL (next two pages).

Start of Figure 7-10

Form1.cs Visual C# Source File

```
using System;
using System.Collections.Generic;
using System.ComponentModel;
using System.Data;
using System.Drawing;
using System.Linq;
using System.Text;
using System.Windows.Forms;

namespace Build_it
{
   public partial class Form1 : Form
   {
      public Form1() { Initialize Component(); }

      private void VKP(object sender, KeyEventArgs e)
      {
         bool isNumberKey = e.KeyCode >= Keys.D0 && e.KeyCode <= Keys.D9;
         bool isPadKey = e.KeyCode >= Keys.NumPad0 && e.KeyCode <= Keys.NumPad9;
         bool isDelKey = e.KeyCode == Keys.Delete || e.KeyCode == Keys.Back;
         if (!(isNumberKey || isPadKey || isDelKey )) e.SuppressKeyPress = true;
      }
      private void button1_Click(object sender, EventArgs e)
      {
          float min, er, theta, max, l4, fc,deltt, u;
          try
          {
             min = float.Parse(textBox3.Text);
             theta = float.Parse(textBox2.Text);
             er = float.Parse(textBox4.Text);
          }
          catch (Exception) { return; }
```

```
1
2               u = (float)Math.Sqrt(er);
3               fc = (float)90.0 * min / theta;
4               l4 = (float)2.94216 / (fc * u);
5               max = ((float)180 - theta) * fc / (float)90;
6               deltt = l4 * u / (float)1.1808e-2;
7
8               textBox1.Text = string.Format("{0:F3}", min);
9               textBox6.Text = string.Format("{0:F1}", deltt);
10              textBox5.Text = string.Format("{0:F3}", max);
11              textBox7.Text = string.Format("{0:F4}", l4);
12
13           }
14          private void textBox2_TextChanged(object sender, EventArgs e){ }
15          private void label2_Click(object sender, EventArgs e) { }
16          private void label6_Click(object sender, EventArgs e) { }
17          private void exitToolStripMenuItem_Click(object sender, EventArgs e) { Application.Exit(); }
18
19          private void button2_Click(object sender, EventArgs e)
20          {
21             textBox3.Text = textBox5.Text;
22          }
23       }
24   }
25
```

Figure 7-10. TRL Line Length Calculator Source Code

27

7.4.8. TRL Calibration Guidelines (Based on Micro-strip MEG6 Stack-up)

The location of the Fixed connector under test is defined as the point at which the trace touches the pad of the Fixed connector. The reference plane is 1.27 mm removed from the geometric transition to avoid measurement anomalies caused by ephemeral modes that result from the change in geometry at the trace to pad transition. Delay times and secondary lengths, shown below, are based on an estimated Dk effective of 2.9 and a 30° phase margin. Actual delay times should be established with TDT measurements of the fixture, with those measurements subsequently used in the TRL calibration, prior to taking measurements.

a) Primary Through Line length is twice the length of the Half-Primary Through Line, shown as 66.57 mm in Figure 7-9.
b) Half-Primary Through Line length is the distance from the launch connector to the reference plane, shown as 33.29 mm in Figure 7-9.
c) Secondary #1 Line length = Primary Through length + 36.57 mm (covers 400 MHz - 2.0 GHz using Megtron-6 stack-up), shown as 103.14 mm, 207.6 ps delay in Figure 7-9.
d) Secondary #2 Line length = Primary Through length + 7.31 mm (covers 2 GHz – 10.0 GHz using Megtron-6 stack-up), shown as 73.89 mm, 41.5 ps delay in Figure 7-9.
e) Secondary #3 Line length = “Primary Through length” + 1.92 mm (covers 10 GHz – 50.0 GHz using Megtron-6 stack-up), shown as 68.04 mm, 8.3 ps delay in Figure 7-9.
f) Short Trace length = one half the length of the Primary Through line length, shown as 33.29 mm in Figure 7-9. The Short Trace is shorted to the GND plane.
g) Load Line length = long line (within reason (e.g., 88.9 mm <= length <= 127 mm)), with two 0201 size 85 Ω resistors (or equivalent, (e.g., 88.7 Ω + 82 Ω)) attached at end of the line, in parallel to ground, shown as 133.15 mm in Figure 7-9.

8

8. OCuLink x4 Cable Connector and Enclosure Labeling

This section specifies the customer-visible labeling. This section builds upon the materials within the *PCI Express Label Specification and Usage Guidelines*. It is critical to keep label size to a minimum while still keeping the fields human readable.

The following attributes are used to construct a cable connector and an enclosure label:

- Signaling: The maximum signaling rate supported by the cable.
  The label *PCIe3* indicates that the maximum signaling rate supported is 8.0 GT/s.
- Link Width: The maximum physical Link width of the connector.
- Peripheral Power: A cable is permitted to support peripheral power.
- Active Cable: A cable is permitted to be implemented as an active cable.
- Vendor-specific Position (VSP): Cable supports vendor-specified positions A12, A13
  - VS (shielded wire attached to VSP positions)
  - VU ((unshielded wire attached to VSP positions)

These attributes are concatenated to construct a cable label as follows:

PCIe3 xLPA

Where:

L is physical number of Lanes provisioned by the cable (1, 2, or 4)

P is the label indicating a cable supports peripheral power

A is the label indicating an active cable

Table 8-1. Examples of Cable Connector and Enclosure Labels

Label	Description
PCIe3 x4P	Passive cable, with four PCI Express Gen 3 Lanes and peripheral power support
PCIe3 x4PA VS	Active cable, with four PCI Express Gen 3 Lanes, peripheral power support and shielded wire attached to the VSP positions
PCIe3 x2P	Passive cable, with two PCI Express Gen 3 Lanes and peripheral power support
PCIe3 x4A VU	Active cable, with four PCI Express Gen 3 Lanes, no peripheral power support and unshielded wire attached to VSP positions
PCIe3 x1P	Passive cable, with one PCI Express Gen 3 Lane and peripheral power support

9

9. OCuLink x4 Implementation Guide

9.1. Enclosure or I/O Bracket Opening for x4 Fixed External Connectors

The minimum opening required for Fixed external OCuLink connectors is shown in Figure 9-1 and Table 9-1 lists the dimensions.

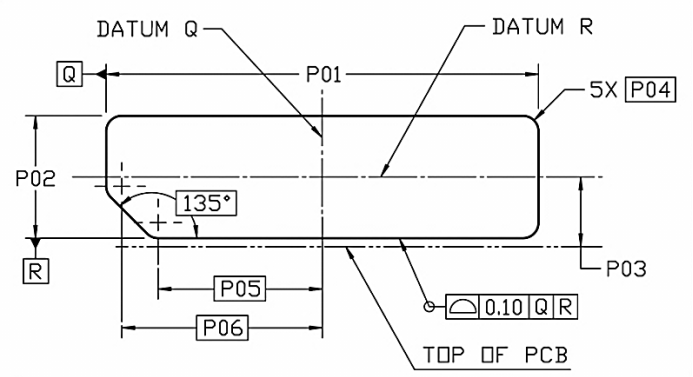


Figure 9-1. Enclosure or I/O Bracket Opening for Fixed External Connector

Implementer is permitted to adjust dimensions, as required, to enable vendor-specific EMI control solution.

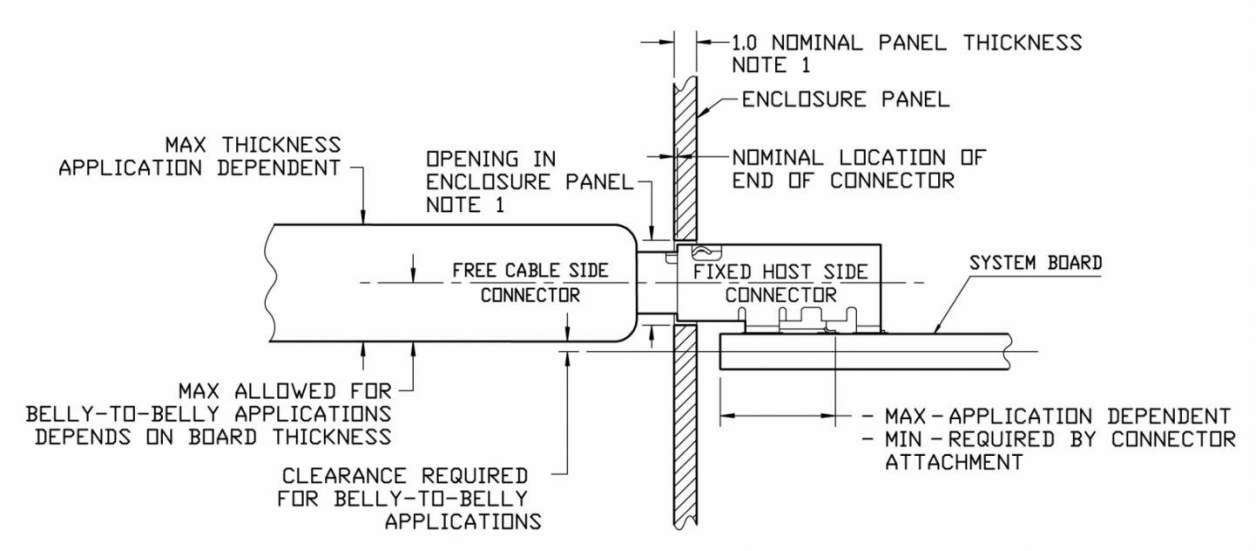
Table 9-1. Dimensions for a Single Fixed External Connector Opening

Designator	Description	Dimension	Tolerance ±
P01	Opening width	13.95	0.08
P02	Opening height	3.93	0.08
P03	Top of PCB to horizontal CL (Datum R) of opening	2.24	0.08
P04	All inside radii	0.50	Basic
P05	Vertical CL of opening (Datum Q) to the lower radius of the orientation feature	5.28	Basic
P06	Vertical CL of opening (Datum Q) to the upper radius of the orientation feature	6.48	Basic

9.2. Clearance Requirements for OCuLink x4 External Connectors and Cables for Enclosures and PCI Add-in Cards

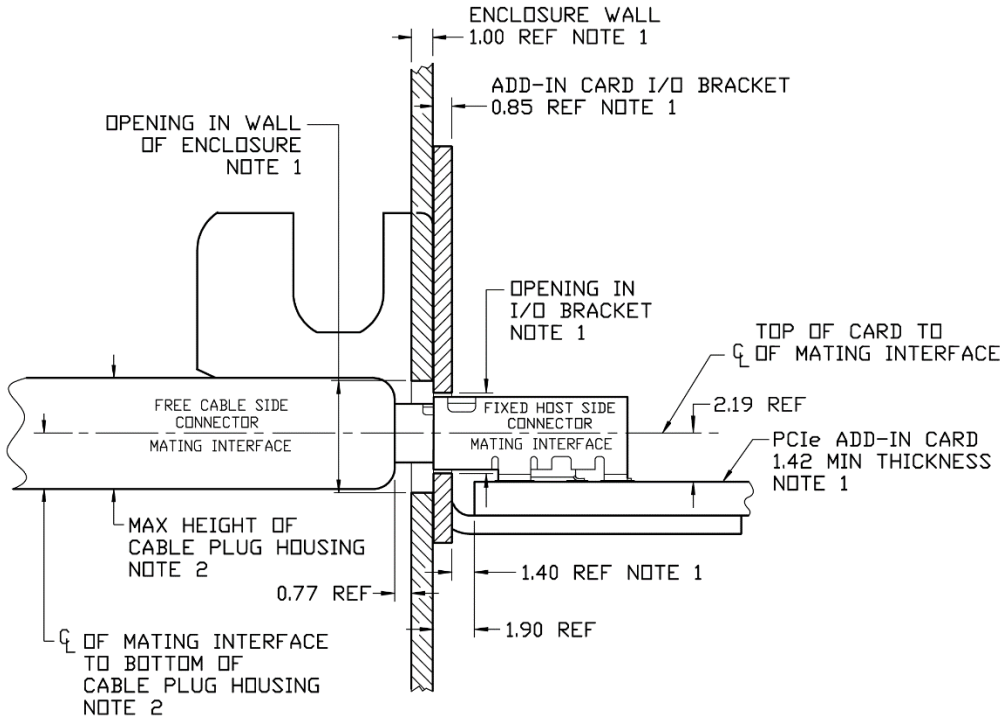
The *PCI Express Card Electromechanical Specification* incorporated requirements that provide clearance for Fixed connectors and Free Cables, implemented in both host/system enclosures and on PCIe add-in cards. The front of the Fixed/host-side connector must be allowed to protrude through the enclosure panel, or through the add-in card bracket by 0.15 mm.

As applications are permitted to utilize different panel thicknesses and/or different distances from the edge of the host board to the inside of the panel, care should be taken in the placement of the Fixed/host connector on the host board (see Figure 9-2) or the add-in card (see Figure 9-3), relative to the edge of the card to maintain the 0.15 mm protrusion.



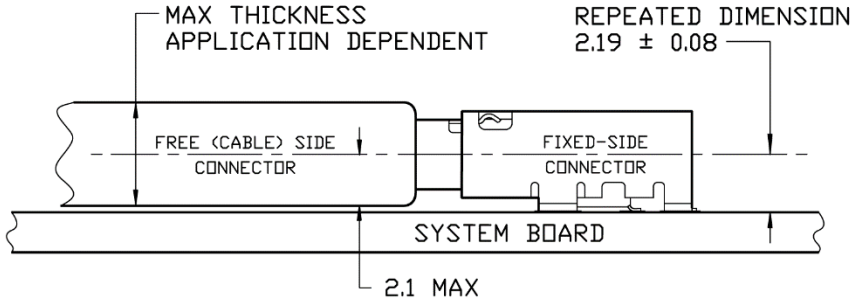
Note: See to the *PCI Express Card Electromechanical Specification* for detailed dimensions.

Figure 9-2. OCuLink x4 External I/O Cable Mated to a Fixed OCuLink Connector on a System/Host Board



Notes:
1: See the *PCI Express Card Electromechanical Specification* for detailed dimensions.
2: Refer to the appropriate Free Cable form factor for dimensions that enable belly-to-belly connections (see Section 6).

Figure 9-3. x4 Free External I/O Cable Mated to a x4 Fixed Host-side Connector on a PCIe Add-in Card Assembled in a System Slot



Note: See the appropriate Free Cable form factor for dimensions that enable connection to a mid-board mounted connector (see Section 6).

Figure 9-4. x4 Internal I/O Cable Mated to a Mid-board Mounted x4 Fixed Host-side Right Angle Connector

A

Appendix A – Cable Management Memory Map

This appendix defines the memory map for the cable management interface. The structure of the map is shown in Figure A-1.

The map is arranged into a single lower page address space of 128 bytes and one mandatory upper address page. Additional upper address pages are not defined in this Specification, but may be used in future expansions.

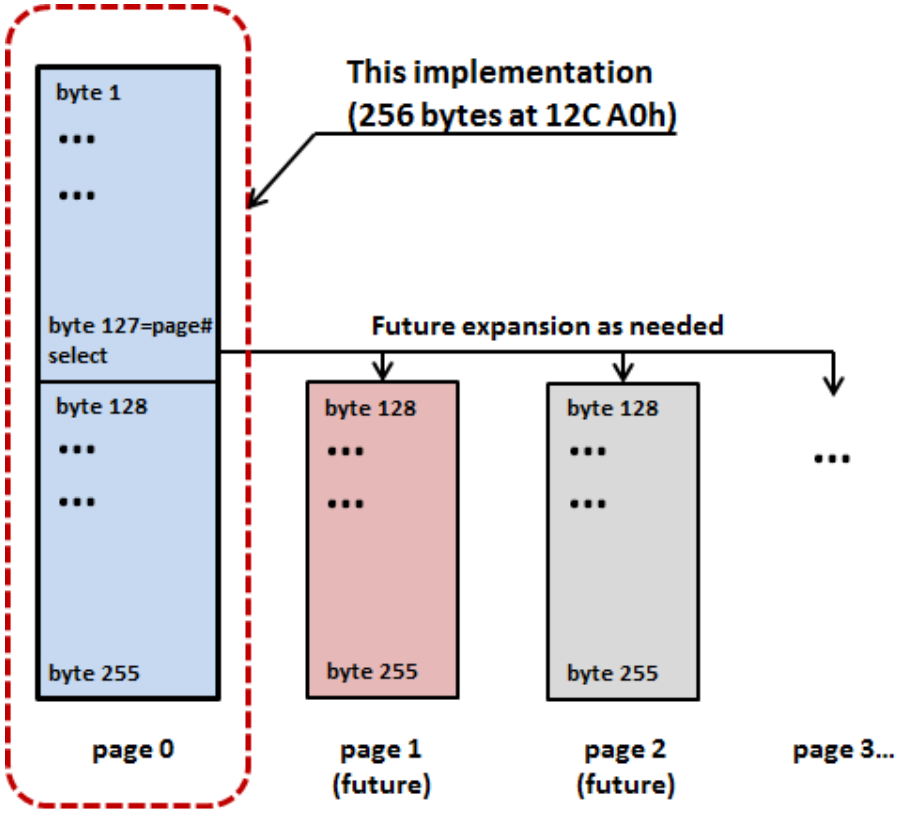


Figure A-1. Cable Management Interface Memory Map

Unless specifically noted, all informative ID fields must contain accurate data. Unless specifically noted, using a value of zero to indicate a field is unspecified is not permitted. Reserved memory locations are to be filled with logical zeroes in all bit locations for reserved bytes, and in reserved bit locations for partially specified byte locations as described in this appendix.

A.1. Lower Page Memory Map

The lower 128 bytes of page 00h are used to access a variety of cable information data. In addition, a mechanism to select upper memory map pages is provided. This portion of the address space is always directly addressable and, thus, is chosen for monitoring and control functions, which may need to be repeatedly accessed.

Table A-1. Bytes 0 to 127 (Lower Memory Fields)

Byte	Description	Value	Type	Notes
0	Identifier	0Eh	Read Only	New Identifier for PCIe
1-2	Status – Flat or paged		Read Only	See Table A-2
3-122	RsvpP			
123	Password entry		Read/Write	Factory access
124	Password entry		Read/Write	Factory access
125	Password entry		Read/Write	Factory access
126	Password entry		Read/Write	Factory access
127	Page Select Byte		Read Only	For future expansion

A.1.1. Identifier

Insert the same identifier value 0Eh into Byte 0 in the lower page (see Table A-1) and Byte 128 in the upper page 00h (see **Table A-3**, Byte 128).

A.1.2. Status

The Status indicator is used to indicate whether flat or paged memory is implemented and is defined in Table A-2.

Table A-2. Status Indicators

Address	Bit	Name	Description
1	All	RsvdZ	
2	0	Flat_mem	Upper memory flat or paged. Flat memory: 0 = paging, 1 = page 00h only
2	1-7	RsvdZ	

A.1.3. Password Change and Entry

Bytes 123-126 are reserved for an optional password entry function.

- Password entry bytes are retained until power down, reset, or rewritten by the Host System.

Additionally, cable vendors are permitted to use this function to implement write protection of Serial ID and other read only information. Password access must not be required to access Free-side device data in either the lower memory page 00h or upper page 00h. Note that multiple manufacturer passwords are permitted to be defined to allow selective access to read or write to various sections of memory, as allowed above.

Host system manufacturer and cable manufacturer passwords must be distinguished by the high order bit (bit 7, byte 123). All Host system manufacturer passwords must fall in the range of 0000 0000h to 7FFF FFFFh, and all cable manufacturer passwords in the range of 8000 0000h to FFFF FFFFh. System manufacturer passwords must be initially set to 0000 1011h in new cables.

A.1.4. Page Select

Byte 127 is used to select the upper page. A value of 00h indicates upper memory page 00h is available to be mapped to locations 128 to 255.

A.2. Upper Page Memory Map

The upper page 00h contains the serial identifiers and is used for read-only identification information. The serial identifier is divided into the base level identifier, extended identifier fields, and vendor-specific data fields. The format of the Serial ID Memory Map is shown in Table A-3.

Table A-3. Upper Page 00h

Byte	Description	Value	Type	Notes
128	Identifier	0Eh	Read Only	New PCIe Identifier
129	Extended Identifier		Read Only	See Table A-4
130	RsvdP			
131	Peripheral Power supported	Bit 0: two Lanes supported 0 = no 1 = yes Bits 7: 1 - RsvdP	Read Only	
132-	RsvdP			

Byte	Description	Value	Type	Notes
138				
139	Number of Lanes	Bits 2:0 001b = 1 Lane 010b = 2 Lanes 100b = 4 Lanes All others RsvdP Bits 7:3 - RsydP	Read Only	Value 3 is not a valid entry for this field
140	Supported PCIe rates	Data Rate Identifier Bit 0 – RsvdP Bit 1 – 2.5 GT/s Data Rate Bit 2 – 5.0 GT/s Data Rate Bit 3 – 8.0 GT/s Data Rate Bits 7:4 – RsvdP.	Read Only	Nominal PCIe Bit Rate; this enables support for Legacy Cables and for future upgrades
141-142	RsvdP			
143 - 144	Propagation delay	16-bit hex number	Read Only	Cable propagation delay (one-way), in nanoseconds
145-146	RsvdP			
147	Cable Technology		Read Only	See Table A-5 and A-6
148 - 163	Vendor Name	ASCII string (16 char)	Read Only	
164	RsvdP			
165-166	PCI-SIG Vendor ID	2 bytes	Read Only	
167	RsvdP			
168-183	Vendor Part Number	ASCII string (16 char)	Read Only	
184-185	Vendor Revision	Hex number (2 bytes)	Read Only	
186-189	Copper Cable Attenuation		Read Only	Copper cable attenuation, in dB, at: 1.25 GHz (Adr 186), 2.5 GHz (Adr 187), 4.0 GHz (Adr 188) and 8.0 GHz (Adr 189); values of all zeroes must be used for an active cable
190	Max. case temp			Maximum case temperature in degrees

Byte	Description	Value	Type	Notes
				Celsius (if unspecified, 70 °C is assumed)
191	Checksum Base	Low order 8 bits of the sum of the contents of bytes 128-190		Checksum of Base ID fields (128-190)
192-195	RsvdP			
196-211	Vendor Serial Number	ASCII string (16 Char)	Read Only	Serial number provided by vendor
212-217	Vendor Date Code	ASCII string (yymmdd)	Read Only	Vendor date code
218-219	Vendor Lot Code		Read Only	Vendor lot code (is permitted to be blank)
220-222	RsvdP			
223	Checksum Extended	Low order 8 bits of the sum of the contents of bytes 192-222		Checksum of Extended ID fields (192-222)
224-255	Vendor Specific Data		Read Only	Vendor-specific data

1

A.3. Extended Identifier

The Extended Identifier is used to identify cable module Power Class and to indicate whether CDRs are present in the module.

Table A-4. Extender Identifier Bits (Address 129)

Bit	Description
Bits 7:6	00b: Power Class Unspecified
	01b: Power Class 1 Cable 0.1 W maximum power consumption
	10b: Power Class 2 Cable 0.6 W maximum power consumption
	11b: Power Class 3 Cable 1.5 W maximum power consumption
5	0: No CDR in TX, 1: CDR present in TX
4	0: No CDR in RX, 1: CDR present in RX
Bits 3:0	RsvdP

A.3.1. Cable Technology

This entry is used to identify cable type.

Table A-5. Cable Technology (Address 147)

Bit	Description
Bits 7:4	Cable Technology (see Table A-6)
Bits 3:0	RsvdP

Table A-6. Cable Technology (Address 147, bits 7:4)

Code	Description of physical device
0h	850 nm VCSEL
1h	1310 nm VCSEL
2h	1550 nm VCSEL
3h	1310 nm FP
4h	1310 nm DFB
5h	1550 nm DFB
6h	1310 nm EML
7h	1550 nm EML
8h	Others
9h	1490 nm DFB
Ah	Copper cable unequalized
Bh	Copper cable passive equalized
Ch	Copper cable, near and far end limiting active equalizers
Dh	Copper cable, far end limiting active equalizers
Eh	Copper cable, near end limiting active equalizers
Fh	Copper cable, linear active equalizers

A.4. Vendor Name

The Vendor Name is a 16-byte field that contains ASCII characters, left-aligned, and padded on the right with ASCII spaces (20h). The Vendor Name must be the full name of the corporation, a commonly accepted abbreviation of the name of the corporation, or the stock exchange code for the corporation. A value of all zeroes in the field indicates that the Vendor Name is unspecified. At least one of the Vendor Name or the PCI-SIG Vendor ID must contain valid non-zero data.

A.4.1. PCI-SIG Vendor ID

This is the 2-byte Vendor ID, allocated by the PCI-SIG. A value of all zeroes indicates that the Vendor ID is unspecified.

A.4.2. Vendor Part Number

The Vendor Part Number is a 16-byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h). This field defines the vendor part number or product name. A value of all zeroes in the field indicates that the Vendor Part Number is unspecified.

A.4.3. Vendor Revision

The Vendor Revision is a 2-byte field that contains ASCII characters, left aligned, and padded on the right with ASCII spaces (20h) and defines the vendor's product revision number. A value of all zeroes in the field indicates that the Vendor Revision is unspecified.

A.4.4. Copper Cable Attenuation

When the cable is identified as passive copper cable (see Table A-3, Byte 147), these bytes will be used to define the cable attenuation. A value of all zeroes indicates that the attenuation is not known or is unavailable.

A.4.5. Vendor Serial Number

The Vendor Serial Number is a 16-byte field that contains ASCII characters, left aligned, and padded on the right with ASCII spaces (20h) and defines the vendor's serial number for the Free-side device. A value of all zeroes in the field indicates that the Vendor Serial Number is unspecified.

B

Appendix B – Management Interface Protocol

B.1. Interface Protocol

In this section, SCL refers to 2-WIRE Clock, while SDA refers to 2-WIRE DATA

B.1.1. Operational States and State Transition

B.1.1.1. Start

A high-to-low transition of SDA with SCL high is a START condition. All bus operations must begin with a START condition.

B.1.1.2. Stop

A low-to-high transition of SDA with SCL high is a STOP condition. All bus operations must end with a STOP condition.

B.1.1.3. Acknowledge

After sending each 8-bit word, the side driving the bus releases the SDA line for one bit time, during which the monitoring side of the bus is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word.

Write data operations must be acknowledged by the slave for all bytes. Read data operations must be acknowledged by the master for all but the final byte read, for which the master must respond with a non-acknowledge (NACK) by permitting SDA to remain high and followed by a STOP.

B.1.1.4. Clock Stretching

To extend the transfer, the slave asserts clock low. This is able to be used by the slave to delay completion of the operation B.1.2 Reset (Management Interface Only).

B.1.2. Reset (Management Interface Only)

To extend the transfer, the slave asserts clock low. This is able to be used by the slave to delay completion of the operation.

B.1.2.1. Power On Reset

The interface must enter a reset state upon loss of power. After power is returned, the interface must transition from the reset state within a time period that is beyond the scope of this document.

B.1.2.2. Protocol Reset

Synchronization issues may cause the master and slave state machines to disagree on the specific bit location currently being transferred, the type of operation, or even if an operation is in progress.

The interface protocol has no explicitly defined reset mechanism. The following procedure may force completion of the current operation and cause the slave to release SDA:

1. The master must provide up to nine SCL clock cycle (drive low, then high) to the slave.
2. The master must monitor SDA while SCL is high on each cycle.
3. If the slave releases SDA, it will be high and the master must initiate a STOP operation.
4. If SDA remains low after a full nine clock cycles, the protocol reset has failed and may need to be repeated.

B.1.3. Format

B.1.3.1. Control

After the start condition, the first 8-bit word of a bus operation must consist of a 7-bit sequence of 101 0000b followed by a read/write control bit.

1	0	1	0	0	0	0	R/W
MSB							LSB

Figure B-1. Control Format

The least significant bit (LSB) indicates if the operation is a data read or write. A read operation is performed if this bit is high and a write operation is executed if this bit is set low. Upon completion of the control word transmission, the slave must assert the SDA signal low to acknowledge delivery (ACK) of the control/address word.

B.1.3.2. Address and Data

Following the read/write control bit, addresses and data words are transmitted in 8-bit words. Data is transferred with the most significant bit (MSB) first.

B.2. Read/Write Operations

B.2.1. Slave Memory Address Counter (Read/Write Operations)

All slaves maintain an internal data word address counter containing the last address accessed during the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the slave. This address remains valid between operations as long as power to the slave is maintained and the slave is not reset. Upon loss of power to or reset of the Free-side device, the slave address counter contents may be indeterminate. The address roll-over during read and writes operations is from the last byte of the 128-byte memory page to the first byte of the same page.

B.2.2. Write Operations (Byte Write)

A write operation requires an 8-bit data word address following the device address write word (1010 0000b) and acknowledgement, see Figure B-2. Upon receipt of this address, the slave must again respond with a zero (ACK) to acknowledge and then clock in the first 8-bit data word. Following the receipt of the 8-bit data word, the slave must output a zero (ACK) and the master must terminate the write sequence with a STOP condition for the write cycle to begin. If a START condition is sent in place of a STOP condition (i.e., a repeated START per the interface Specification), the write is aborted and the data received during that operation is discarded. Upon receipt of the proper STOP condition, the slave enters an internally timed write cycle, t_{wp}, to internal memory. The slave disables its management interface input during this write cycle and must not respond or acknowledge subsequent commands until the internal memory write is complete. Note that interface "Combined Format" using repeated START conditions is not supported on write commands.

		<-OCuLink ADDRESS->									<- MEMORY ADDRESS ->									<- DATA WORD ->									
HOST	START	MSB						LSB	WRITE		MSB							LSB												STOP
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
OCuLink										ACK									ACK	MSB							LSB	ACK	

Figure B-2. Write Byte Operation

B.2.3. Write Operations (Sequential Write)

The slave must support up to a four sequential byte write without repeatedly sending slave address and memory address information as shown in Figure B-3. A sequential write is initiated the same way as a single byte write, but the host master does not send a STOP condition after the first word is clocked in. Instead, after the slave acknowledges receipt of the first data word, the master is able to transmit up to three more data words. The slave must send an “acknowledge” after each data word received. The master must terminate the sequential write sequence with a STOP condition or the write operation must be aborted and data discarded. Note that the interface “combined format” using repeated START conditions is not supported on write commands.

		<-OCuLink ADDRESS->									<- MEMORY ADDRESS ->								
HOST	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0
OCuLink										ACK									ACK
Begin Figure B-3																			

<--- DATA WORD 1 --->									<--- DATA WORD 2 ---->								
MSB							LSB		MSB							LSB	
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0
								ACK									ACK
Figure B-3 Middle																	

<--- DATA WORD 3 --->									<--- DATA WORD 4 ---->									
MSB							LSB		MSB							LSB		STOP
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
								ACK									ACK	
Figure B-3 End																		

Figure B-3. Sequential Write Operation

B.2.4. Write Operations (Acknowledge Polling)

Once the slave internally timed write cycle has begun (and inputs are being ignored on the bus), acknowledge polling is able to be used to determine when the write operation is complete. This involves sending a START condition followed by the device address word. Only if the internal write cycle is complete must the slave respond with an “acknowledge” to subsequent commands, indicating read or write operations is able to continue.

B.2.5. Read Operations (Current Address Read)

A current address read operation requires only the Slave address read word (1010 0001b) be sent, see Figure B-4. Once acknowledged by the Slave, the current address data word is serially clocked out. The transfer is terminated when the Master responds with a NACK and a STOP instead of an “acknowledge”.

		<--OCuLink ADDRESS-->																	
HOST	START	MSB						LSB	READ									NACK	STOP
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
OCuLink										ACK	MSB							LSB		
											<---- DATA WORD ----->									

Figure B-4. Current Address Read

B.2.6. Read Operations (Random Read)

A random read operation requires a dummy write operation to load in the target byte address as shown in Figure B-5. This is accomplished by the following sequence: the target 8-bit data word address is sent following the device address write word (1010 0000b) and acknowledged by the slave. The master then generates another START condition (aborting the dummy write without incrementing the counter) and a current address read by sending a device read address (1010 001b). The slave acknowledges the device address and serially clocks out the requested data word. The transfer is terminated when the master responds with a NACK and a STOP (instead of an "acknowledge").

		<-OCuLink ADDRESS->									<- MEMORY ADDRESS ->								
HOST	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0
OCuLink										ACK									ACK
Begin Figure B-5																			

	<-OCuLink ADDRESS->																		
START	MSB						LSB	READ										NACK	STOP
	1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
									ACK	MSB							LSB		
										<---- DATA WORD n---->									
Figure B-5 End																			

Figure B-5. Random Read

B.2.7. Read Operations (Sequential Read)

Sequential reads are initiated by either a current address read (see Figure B-5) or a random address read (Figure B-6). To specify a sequential read, the master responds with an “acknowledge” (instead of a STOP) after each data word.

		<-OCuLink ADDRESS->																	
HOST	START	MSB						LSB	READ										ACK
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	0
OCuLink										ACK	MSB							LSB	
											<---- DATA WORD n---->								
Begin Figure B-6																			

								ACK									NACK	STOP	
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1		
MSB							LSB		MSB							LSB			
<-- DATA WORD n+1 --->									<-- DATA WORD n+x --->										
Figure B-6 End																			

Figure B-6. Sequential Address Read Starting at Current Address

As long as the slave receives an “acknowledge”, it must serially clock out sequential data words. The transfer is terminated when the master responds with a NACK and a STOP instead of an “acknowledge”.

		<-OCuLink ADDRESS->									<- MEMORY ADDRESS ->								
HOST	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0
OCuLink										ACK									ACK
Begin Figure B-7																			

	<-OCuLink ADDRESS->																	
START	MSB						LSB	READ										ACK
	1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1
									ACK	MSB							LSB	
										<---- DATA WORD n---->								
Figure B-7 Middle																		

								ACK									NACK	STOP
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1	
MSB							LSB		MSB							LSB		
<-- DATA WORD n+1 --->									<-- DATA WORD n+x --->									
Figure B-7 End																		

Figure B-7. Sequential Address Read Starting with Random Read

B.3. Timing Diagram

The timing diagram for the interface is shown in Figure B-8 and the timing parameters are specified in Table B-1.

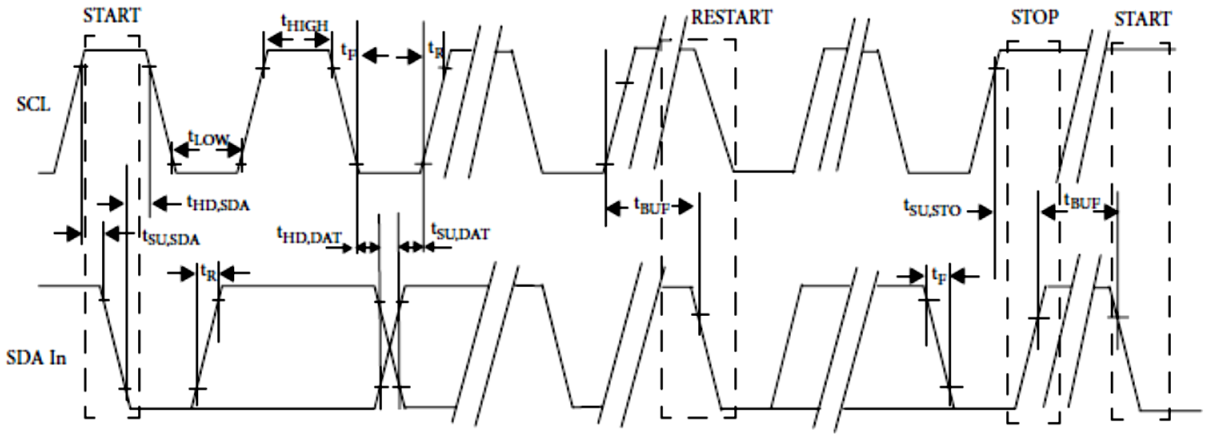


Figure B-8. Cable Management Interface Timing Diagram

Table B-1. Timing Parameters

Parameter	Symbol	Min	Max	Unit	Conditions
Clock Frequency	f_{SCL}	0	400	kHz	
Clock Pulse Width Low	t_{LOW}	1.3		µs	
Clock Pulse Width High	t_{HIGH}	0.6		µs	
Time bus free before new transmission is able to start	t_{BUF}	20		µs	
START Hold Time	$t_{HD,SDA}$	0.6		µs	
START Set-up Time	$t_{SU,SDA}$	0.6		µs	
Data In Hold Time	$t_{HD,DAT}$	0		µs	
Data in Set-up Time	$t_{SU,DAT}$	0.1		µs	
Input Rise Time (400 kHz)	$t_{R,400}$		300	ns	
Input Fall Time (400 kHz)	$t_{F,400}$		300	ns	
STOP Set-up Time	$t_{SU,STO}$	0.6		µs	

B.4. Non-Volatile Memory Specification

The memory transaction timings are given in Table B-2.

Table B-2. Non-Volatile Memory Specification

Parameter	Symbol	Min	Max	Unit	Conditions
Complete Single or Sequential Write	t_{WP}		40	ms	Complete (up to) 4-byte Write
Serial Interface Clock Holdoff (Clock Stretching)	$t_{SCL,HOLDOFF}$		500	µs	Maximum time the cable module is permitted to hold the SCL line low before continuing with a read or write operation
Endurance (Write Cycles)		50,000		Cycles	70 ºC

C

Appendix C – External Cable Power Requirements

The requirements when implemented are:

- Optional Peripheral Power from the root only supports up to 10 W MAX, equally divided on the two 5 V pins.
- Root devices that provide optional peripheral power are responsible for preventing reverse current flow.
- In a tethered configuration where peripheral 5 V power is supplied by the Root, V_{act} at the end point is included in the root 10 W budget.
- All OCuLink enclosures must support V_{act} (1.5 W Max per defined pins).
  - V_{act} must be provisioned per connector end.
    (i.e., V_{act} is not carried through the cable from the root to the end point).
  - V_{act} must remain “on” in all power management states.
  - Required to support cable management services.

To avoid exceeding system power supply limits and cooling capacity, all cables at power up, by default, must operate with ≤1.5 W. The maximum power level is allowed to exceed the classified power level for 500 ms, following hot insertion or power up. However, the current is limited to values given by Table C-1 and illustrated in Figure C-1.

At host power up the host must supply 3.3 V_{act} TX and 3.3 V_{act} RX to the cables within 100 ms of each other. Table C-1-1 is swept from 10 Hz to 10 MHz, according to the methods of C.3.3. This emulates the worst case noise of the host.

It is also desirable for a cable and host to each tolerate a degree of random or semi-random noise on both 3.3 V_{act} TX and 3.3 V_{act} RX, simultaneously, but the characteristics of this noise are beyond the scope of this document.

1

Table C-1. OCuLink Cable Assembly Power Requirements

Parameters	Symbol	Conditions	Min	Max	Units
Power supply noise tolerance including ripple [peak-to-peak]				66	mV
Power supply voltages including ripple, droop and noise below 100 kHz	3.3 V_{act} TX 3.3 V_{act}t RX	Note 1	3.14	3.46	V
Instantaneous peak current at Hot-Plug		Note 2, 3		400	mA
Sustained peak current at Hot-Plug		Note 2, 3, 5		330	mA
Instantaneous peak current on enabling		Note 2, 3, 5		600	mA
Sustained peak current on enabling		Note 2, 3 , 5		500	mA
Maximum power consumption		Note 4		1.5	W
Maximum power consumption at power up		Note 4		1.5	W

Notes:

1. Set point is measured at the input to the connector on the host board reference to ground.
   Droop is any temporary drop in voltage of the power supply, such as that caused by plugging in another cable assembly or when enabling another cable assembly.
2. The requirements for current apply to the current through each inductor.
3. The maximum currents are the allowed currents for each power supply; therefore, the total module peak currents are permitted to be twice this value. The instantaneous peak current is allowed to exceed the specified maximum current capacity of the connector contact for a short period, see Figure C-1.
4. Maximum cable assembly power consumption must not exceed 1.5 W from 500 ms after power up.
5. Not to exceed the sustained peak limit for more than 50 us; but is permitted to exceed this limit for shorter durations.

2

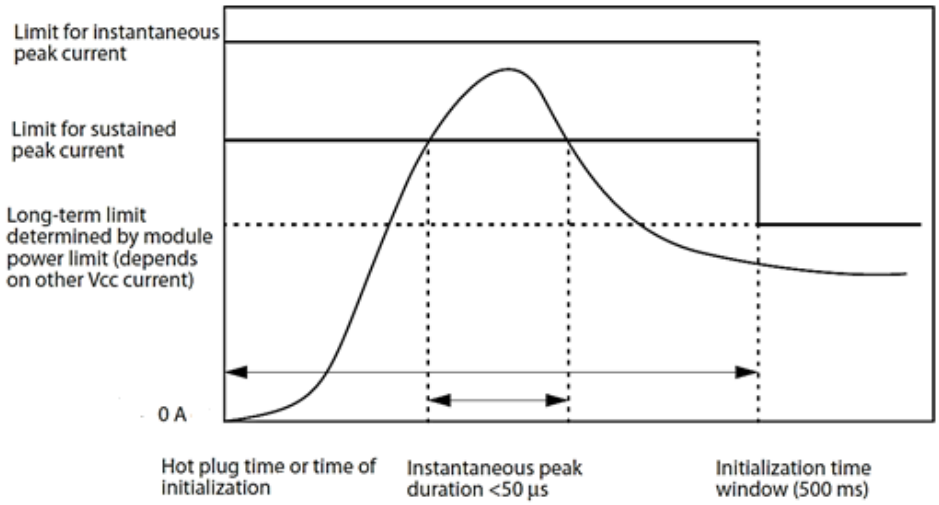


Figure C-1. Instantaneous and Sustained Peak Current for 3.3 V_{act} TX and 3.3 V_{act} RX

C.1. Power Sequencing

There is no specific requirement for power supply sequencing of each of the two power supply rails. They are permitted to come up or go down in any order. The system, however, must assert the PERST# signal whenever either of the two power rails go outside of the specifications.

C.2. Power Decoupling

Due to the low level signaling of the PCI Express interface, it is strongly recommended that sufficient decoupling of all power supplies be provided. This is recommended to ensure that power supply noise does not interfere with the recovery of data from a remote Upstream PCI Express device.

D

Appendix D - System and Link Electrical Characteristics

Additional Electrical performance characteristics are to be addressed by the two system boards with Fixed OCuLink connector Ports. They, along with an OCuLink cable assembly, form the complete solution Link. These characteristics include:

- AC-coupling capacitors
- Lane-to-Lane skew
- Transmitter Equalization
- Skew within a differential pair
- Differential data trace impedance
- Differential data trace propagation delay

The electrical budgets include each of the three Link components:

- Cable Assembly with OCuLink Free connectors
- Two (2) System boards with OCuLink Fixed connectors

The interconnect Link budget allocations associated with the Transmitters and Receivers differ to account for any electrical characteristics the AC coupling capacitors may contribute to the Link.

It is recommended that the electrical impact of discontinuities (via, bend, test-points, etc.) on the Link be included in the respective components.

D.1. AC Coupling Capacitors.

The PCI Express system boards must incorporate AC coupling capacitors on the Transmitter differential pair. This is to ensure blocking of the DC path between two OCuLink PCI Express systems boards. The specific capacitance values are specified in the *PCI Express Base Specification*.

Note: Attenuation or jitter caused by the coupling capacitors must be accounted for as part of the budget allocation for the physical interconnect component's path on which the capacitors are mounted. Note that there may be parasitic effects associated with the component's placement as mounted on the printed circuit board.

D.2. Crosstalk

All system board designs must properly account for any crosstalk that may exist among the various pairs of differential signals. Crosstalk may be either near-end (NEXT) or far-end (FEXT). Each component has potential impact on a design and must be planned for accordingly.

Crosstalk between differential pairs influences and impacts the data signals and any subsequent loss and jitter budgets. Note that all eye diagrams must account for any and all crosstalk present in order to limit crosstalk impacts and implications.

All system boards interfacing with a cable assembly must also properly account for crosstalk. The system board must also account for potential crosstalk that occurs on the printed circuit board as well as within the connector itself.

D.3. Transmitter Equalization

For system boards that support 8.0 GT/s signaling, refer to the *PCI Express Base Specification* for equalization preset requirements. A system board must meet eye diagram requirements at 8.0 GT/s on each Lane with one or more preset equalization settings.

The cable Port must meet the following additional rules for this Specification:

- The Upstream and Downstream Transmitters must be configured based on the data stored in the cable management memory. Receivers are also permitted to be set using this information.

D.4. Skew within the Differential Pair

The skew within the differential pair gives rise to a common-mode signal component, which can, in turn, increase Electromagnetic Interference (EMI). The system board differential pairs must be routed such that the skew within differential pairs is ≤ 10 ps / 1 m and pair-to-pair is ≤ 40 ps / 1 m.

D.5. Differential Data Trace Impedance

The PCB trace pair differential impedance for an 8.0 GT/s capable data pair must be in the range of 70 Ω to 100 Ω (85 Ω with a relative tolerance of ± 7%).

Note: This requirement does not apply to vias, the connectors, package traces, cables, and other similar structures.

Designs should still attempt to minimize the impedance discontinuities from vias, the connectors, package traces, cables, and other similar structures.

D.6. Differential Data Trace Propagation Delay

The propagation delay for a system board data trace from the Fixed connector to the Receiver/Transmitter must not exceed 4.9 ns.

Appendix E - Active Cable Assemblies

- External Host Board-side Cable interfaces intended to operate at PCIe Gen 3 (8.0 GT/s) must be designed to support both passive and active cables.
- Active cables must contain memory.
- Each cable manufacturer is responsible for:
  - Creating and storing data in a method consistent with Appendix A and Appendix B.
  - Ensuring that the Link is able to operate when using the eye diagrams defined in *PCI Express Base Specification,* and other *PCI Express Specifications* listed in Section 1.1 Reference Documents.
- Active cable behavior must take into account Link training protocol specified in the *PCI Express Base Specification,* and be able to accept the potential changes from the Subsystem Transmitters during Link training at 8.0 GT/s.
- Active cables must initially operate at 2.5 GT/s in order to ensure initial Link training and then operate at the highest Link speed supported.
- Must transparently support Electrical Idle and Receiver Detect.
- Permitted to support arbitrarily long cable lengths as constrained by the active component power budget and PCI Express clocking schemes in specific applications.
- Permitted to be visible to enclosure software as required for identification and management purposes.
- Active cables require both the ROOT and ENDPOINT to provide 3.3 volts.
- Only the ROOT supplies 5 volts to power endpoint (downstream) devices.
- The use of SMBus across the cable is an optional feature. This allows the use of cables that adhere to SFF-8449, for a PCI Express interface with a reduced feature set. Active Optical Cable assemblies may not want to implement SMBus across the cable for cost or complexity reasons, and therefore are permitted to have a reduced feature set. The Upstream Subsystems should not be designed in such a way as to require the use of SMBus across the cable. However, the SMBus controller is still required, by both Upstream and Downstream fixed ends, to read the cable assembly information for configuration of the PCIe devices that are part of the cabled Link.
- It is the system implementer's responsibility to meet the electrical Specifications for the SMBus, when used across the cable.
- The External OCuLink interface must be designed to meet applicable safety standards. Usually, this means that a powered connection implements current limiting on any devices connected to the interface. Two examples are:
  - Active cables
  - Power delivery to Downstream endpoint ports.

Appendix F – System Level Port Aggregation

- The Upstream device needs to have Lanes configured into Ports of the desired size and configuration before Link training is able to begin. The method in which this occurs is beyond the scope of this Specification.
- The Upstream Subsystem and Downstream Subsystem must read the cable management Memory Space to determine how each physical cable interface should be configured. However, if the lowest order Cable Port is identified to be a x16, it is permissible to ignore the other Ports.
- The method for reading each Port is implementation specific. The sideband signals for the lowest order cable Port must represent the logical Link and it is permissible to ignore the higher order cable Port sidebands.
- The cable management controller must configure each Port individually, regardless of the logical Port width.

G

Appendix G – Acknowledgements

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Company affiliation listed is at the time of Specification contributions.